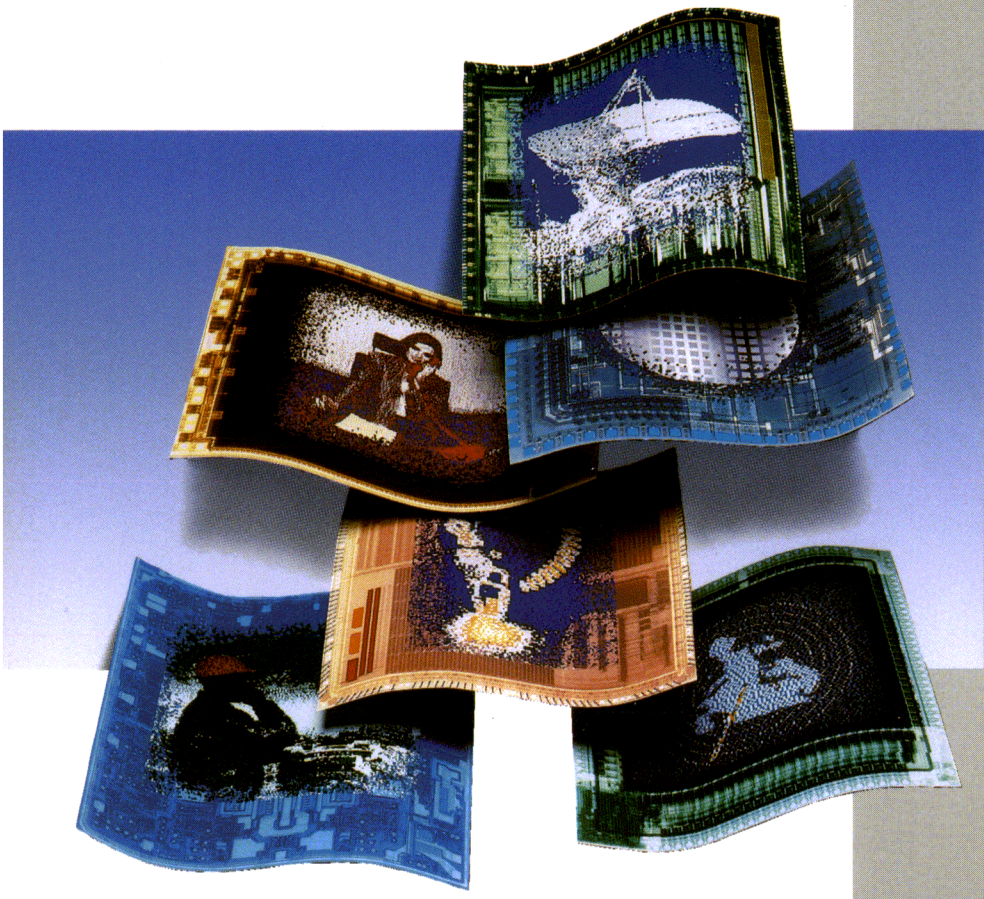
Global Positioning

Products Handbook

August 1996



GEC PLESSEY
SEMICONDUCTORS

DATASHEET ANNOTATION

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TARGET SPECIFICATION

This is the most tentative form of information and represents a very preliminary product specification. No actual design work on the product has started.

PRELIMINARY INFORMATION

The product is in design and development. The datasheet represents the product as it is understood but details may change.

ADVANCE INFORMATION

The product design is complete and final characterisation for volume production is well in hand.

No annotation

The product parameters are fixed and the product is available to datasheet specification in volume.

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GEC PLESSEY
SEMICONDUCTORS

GLOBAL POSITIONING

Products Handbook

GEC PLESSEY
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Foreword

GEC Plessey Semiconductors has a world-class reputation for ICs for radio frequency applications. The company offers ICs for global positioning systems (GPS) together with development systems to assist GPS Receiver design.

Originally supplying a range of radio parts such as amplifiers, synthesisers and prescalers, GEC Plessey Semiconductors has developed and enhanced its technologies to suit much higher system integration, and now offers some of the most advanced integrated circuits available, providing cost effective, high performance solutions for emerging GPS receiver applications.

GEC Plessey Semiconductors is one of very few companies with the complete range of semiconductor technology for the integration of a GPS receiver.

- leading edge RF bipolar technologies with on-chip capacitors and inductors
- CMOS for digital signal processing (including 12 channel correlators and support functions)
- ARM 32-bit RISC microprocessor
- SAW Filter technology
- advanced packaging techniques

With these, and with many years experience of implementing systems on silicon, GEC Plessey Semiconductors is well placed to support your IC requirements for GPS.

This Global Positioning Products Handbook details some of the latest development in chipsets for GPS receivers. Take a look at what's in here and give us a call !

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Product List - alpha numeric

Section 1

GP2000 Designer's Guide

GEC PLESSEY

SEMICONDUCTORS

GP2000

GLOBAL POSITIONING CHIPSET – DESIGNER'S GUIDE

The GP2000 chipset comprises the GP2010 RF front end and the GP2021 12-channel correlator. Together with a microprocessor and a SAW filter (both available from GEC Plessey Semiconductors) these two circuits form the heart of a GPS (Global Positioning System) Receiver. This designer's guide provides technical information on the GP2000 chipset, on GPS systems in general and on the GPS Builder-2™ development kit.

PRACTICAL RECEIVER IMPLEMENTATION

A typical GPS receiver is shown in Fig. 1. From the antenna, the signal is down-converted by the front end circuit ready for processing by the correlator. A microprocessor controls the receiver operation, including interfacing to any external display or other function.

SUBSYSTEM SELECTION ISSUES

Microprocessor Selection

It is difficult to state a minimum specification for a microprocessor suitable for use in a GPS receiver since the choice is influenced by many factors.

The performance requirements are dictated by the application and functionality of the receiver as a whole and possibly by the system of which the receiver is a part.

For volume GPS applications the trend is towards higher levels of integration. As a consequence there is a need to share resources with other parts of the complete system.

The microprocessor may be required to perform processing of tasks which are not directly related to producing a position fix, such as control of devices peripheral to the receiver.

Spare processing power, after catering for the GPS specific tasks, is an attractive feature for providing cost reductions by the possible removal of other microprocessors.

Normally, the microprocessor is required to perform both integer and floating point arithmetic, although floating point calculations will usually be constrained to the navigation solution procedures.

The use of a maths co-processor is usually precluded for cost reasons but may be unavoidable if, for instance, a high solution update rate is required (many times a second).

Processor loading can be traded-off against the number of active channels. However, retrospectively, this may have an adverse impact on the software complexity and navigation performance.

The familiarity of the developers with the development platform and the suitability of the available tools for the development of real-time embedded applications is also important.

Memory Selection

The memory requirements of the GPS receiver should be carefully considered since this constitutes a large portion of the component costs. The choice of memory can be complex and trade-offs need to be made against component costs, speeds and power consumption. As with the choice of microprocessor, the size of memory required by the receiver is also application specific.

However, typical memory sizes, when considering just the GPS software, are 256 Kbytes of ROM and 64 Kbytes of RAM. (These figures are for a production engine: a development system is likely to need more memory).

Memory savings by the reduction of the number of active channels are not necessarily significant.

Some non-volatile memory (NVM) may be required for information retention during periods of power-down. Parameters such as time-to-first-fix (TTFF) can be substantially improved by retaining satellite almanacs, ephemerides, reference oscillator characteristics and other data in the NVM. Typical NVM requirements amount to about 8 Kbytes.

The choice of RAM type may be influenced by software throughput requirements.

Time critical portions of code may be run from fast SRAM (zero wait state) at the expense of memory cost and power consumption.

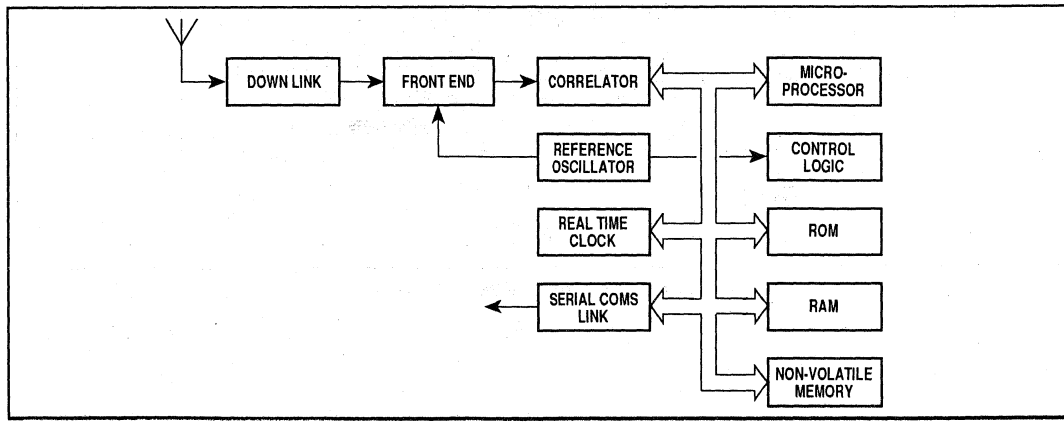


Fig. 1 Generic GPS receiver

The choice of microprocessor may influence memory selection if it has desirable features such as an on-chip cache RAM.

Reference Oscillator

The reference oscillator can be a significant cost component in a GPS receiver.

The short-term stability tends to impact on the receiver tracking performance since it is equivalent to the receiver undergoing a change in dynamics.

The long-term stability tends to impact signal acquisition times and receiver TTFF since it can widen the acquisition search window and increase the window overlap.

The main trade-offs for reference oscillator selection are between cost, stability and temperature range.

Careful consideration should be given to the operating temperature range due to its relationship to oscillator cost (a wider temperature range for a given stability means a higher cost) and stability (a narrower temperature range for a given stability at lower cost).

Temperature compensated crystal oscillators (TCXOs) of stabilities in the region ±3ppm over a temperature range of approximately −30°C to +70°C provide a good general purpose oscillator. They can give acceptable performance even without software characterisation of the oscillator (prediction of the oscillators offset from its nominal value).

Cheaper, less stable (±10ppm or so) uncompensated crystal oscillators can be used in conjunction with software characterisation and compensation and still give the required performance over a wide operating temperature range.

The designer should be aware if the type of oscillator used is prone to any sudden step changes in stability over the operating range since such characteristics are likely to cause loss of signal tracking.

Other Blocks

Real-Time Clock

The use of a real-time clock, if kept active during power-downs, can shorten acquistion times by enabling prediction of satellite visibilities and Doppler shifts. This reduces the TTFF by enabling a 'warm' start.

Serial Communications

Most GPS engines will have at least two serial I/O ports. One is usually dedicated to the reception of RTCM SC-104 DGPS correction data and the other for receiver control and status monitoring.

Control Logic

Dependent upon the exact nature of the receiver components, a certain amount of control or glue logic may be necessary to interface the components together.

GP2010/GP2021/ARM60 GPS RECEIVER

Fig. 2 shows how the GP2010, GP2021 and ARM60 can be used to create a low cost GPS receiver solution with 12 channels and a minimum of external supporting components.

The internal memory management control logic of the GP2021 means that when used with the ARM60 no additional control or glue logic is required.

The GP2021 supports RAM, E^2PROM and ROM/EPROM/FLASH with a configurable number of wait states for the E^2PROM and ROM.

The on-chip real-time clock (RTC) and dual UART functions reduce the need for external components still further.

The GP2010 and GP2021 integrated circuits are described in the following two sections

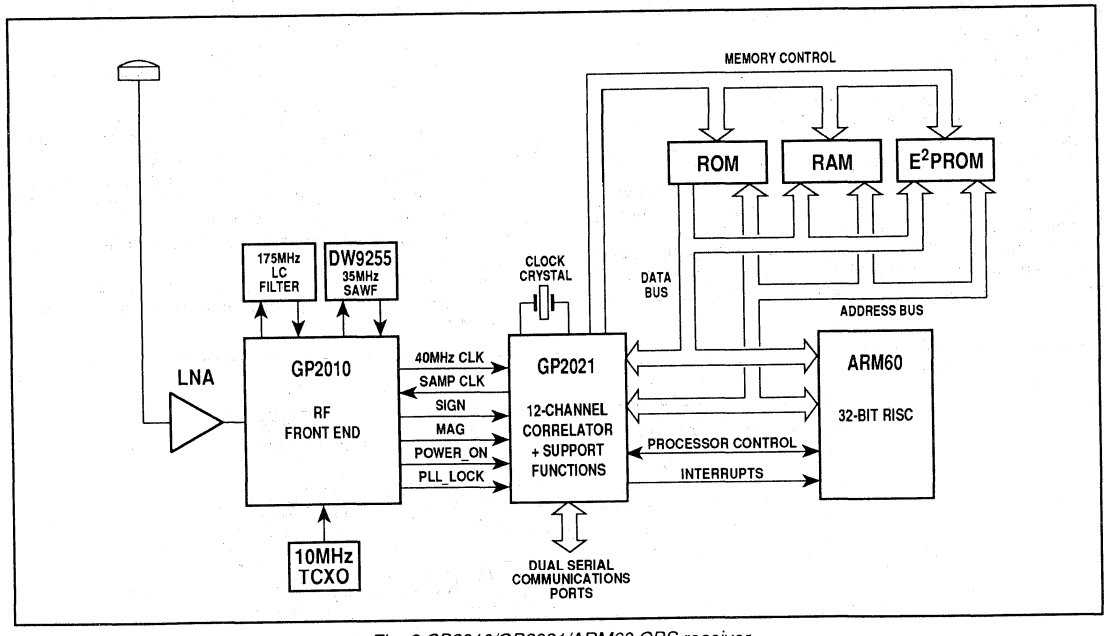


Fig. 2 GP2010/GP2021/ARM60 GPS receiver

GP2010 RF FRONT END

FEATURES

- L1 C/A Code Front End
- Low Voltage Operation (3V to 5V)
- Low Power Consumption (200mW at 3V)
- On-chip Phase Locked Loop including VCO
- 3-Stage Down Conversion
- 2-Bit Digital Output (Sign and Magnitude)
- −40°C to +85°C Operating Temperature Range
- Interfaces to GP2021 Digital Correlator
- Few External Components Required

FUNCTIONAL OVERVIEW

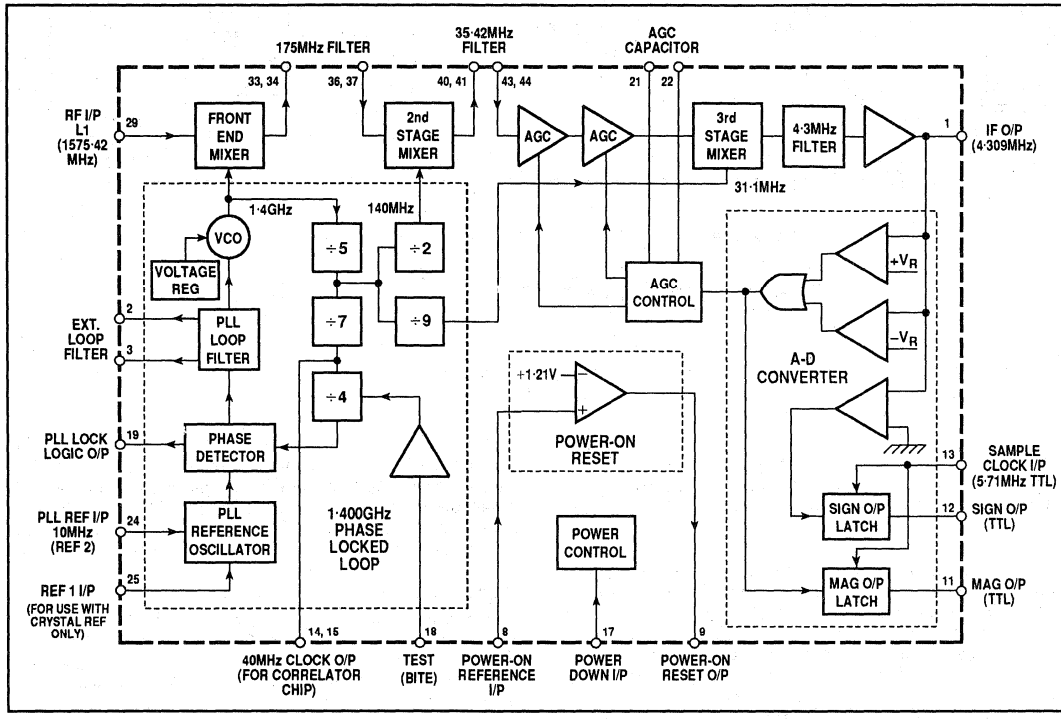


Fig. 3 GP2010 block diagram

Fig. 3 is a block diagram of the front end integrated circuit GP2010.

Several key blocks can be identified:

- On-Chip Phase Locked Loop
- Triple Down-Conversion
- AGC
- Power Control

On-Chip Phase locked Loop

An on-chip Phase Locked Loop (PLL) requiring only an external 10MHz reference (0·1 to 1·2V p-p) synthesises 1400MHz which is used to generate all intermediate frequency local oscillators for signal down-conversion. These frequencies are 1400MHz, 140MHz and 31·111MHz. An external 40MHz clock (for use by the GP2021 correlator) is also generated. This signal is low level differential to minimise interference.

The design has been implemented to minimise the number of external components. The application circuit (Fig. 4) shows the components required.

The Voltage Controlled Oscillator (VCO) has an on-chip voltage regulator to improve noise immunity of the PLL (only available in 5V operation).

Signal Down-Conversion

First Stage

The first stage of signal down-conversion mixes the L1 signal at 1575·42MHz with a local oscillator at 1400·0MHz to give a first IF of 175·42MHz. This places the image at 1224·58MHz (i.e. approximately L2)

The high first IF means that image attenuation can be easily achieved with a combination of a selective antenna and a simple low-cost filter at the antenna or input to the front end.

The first stage mixer has an image rejection filter of about 5dB (minimum) and 1dB compression point of −22dBm (minimum). Together with the selective antenna and RF filter, this provides a good level of protection against saturation at the input from out-of-band interfering signals.

The first IF filter is also used to suppress interfering signals near to the IF to prevent saturation of the second stage mixer.

In practice, a typical first IF filter can be realised with discrete components as, for example, a 2-pole coupled-tuned filter, where a bandwidth of about 20MHz is achievable.

Second Stage

The second stage of signal down-conversion mixes the signal at 175·42 MHz with a local oscillator at 140·0 MHz to give a

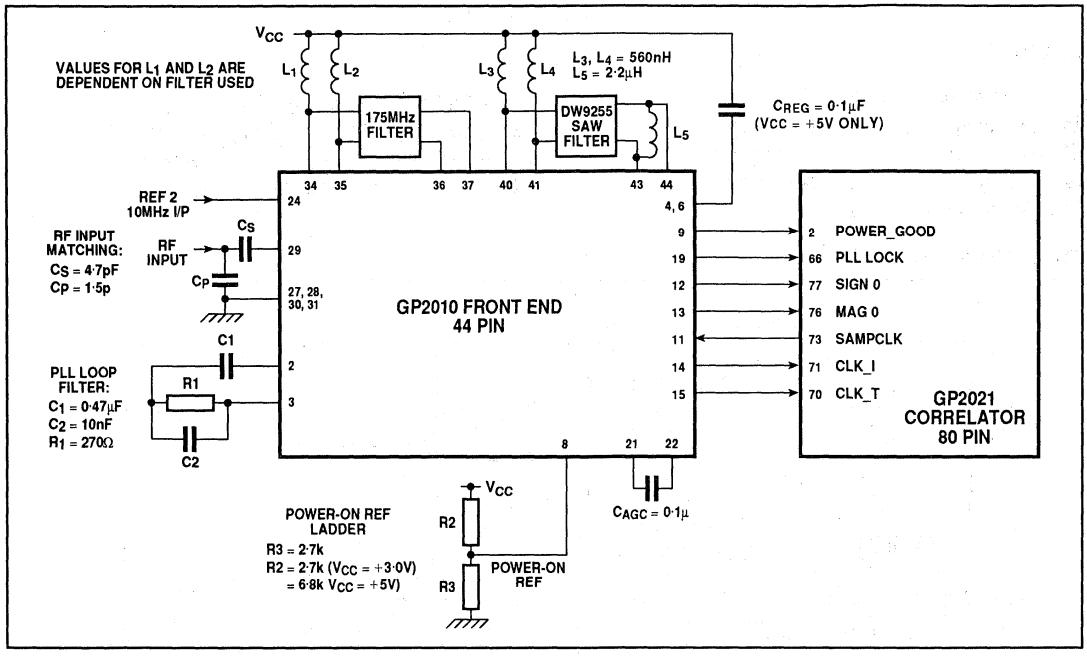


Fig. 4 Application circuit

second IF of 35·42 MHz. This places the image at 104·58MHz.

Attenuation of the image is achieved via use a 175·42MHz bandpass (±1MHz) filter before the second stage mixer. This complements any image attenuation at this frequency from the antenna and RF filter.

Third Stage

The third stage of signal down-conversion mixes the signal at 35·42MHz with a local oscillator at 31·111MHz to give a third IF of 4·309MHz, placing the image at 26·802MHz.

The second IF filter is critical to system performance and effectively sets the bandwidth of the front end. To achieve high levels of image and interference rejection, a filter with a very tight passband and sharp cut-off is required.

The use of a SAW filter, such as the GEC Plessey Semiconductors DW9255, is recommended to achieve these types of characteristic. The DW9255 has a 1·9MHz passband centred on 35·42MHz with 0·8dB of passband ripple and out-of-band rejection of better than 21dB at ±2·0MHz and better than 35dB at ±7·5MHz.

AGC and Sampling

Following the third stage mixer the signal is filtered with an on-chip 4·3MHz passband (±1MHz) filter. The signal is then used to control the gain of the AGC which appears between the second IF filter and third stage mixer (Fig. 5). The AGC caters for factors such as varying RF amplifier gain and cable loss.

The AGC operates such that the magnitude bit (MAG) at the output of the 2-bit A-to-D converter is high for nominally 30% of the time. When the magnitude bit is high it is given a value of 3. When low it is given a value of 1. The SIGN bit will be high for nominally 50% of the time. This statistical distribution of data aids the system in suppressing CW interference.

Signal Down-Conversion Sampling

The signal at its third IF of 4·309MHz is then sampled and latched at the SIGN and MAG outputs. When used with the GP2021 the sampling clock is at 5·714MHz. The aliasing present in the sampling process produces a final digital signal at an IF of nominally 1·405 MHz (Fig. 6).

Power Supplies

The analog and digital sections of the device can be operated from separate power supplies to prevent interaction with digital switching transitions in the analog section.

The GP2010 includes an on-chip voltage detector for the digital supply. This drives a logic output which goes high when the power supply has reached a nominal value. This output can be used to disable the correlator and microprocessor when power supply switching is occurring.

The GP2010 can be put into a Power-Down mode where most of the device, except the power supply switching detector, is disabled. This changes the current consumption from nominally 70mA to 10mA.

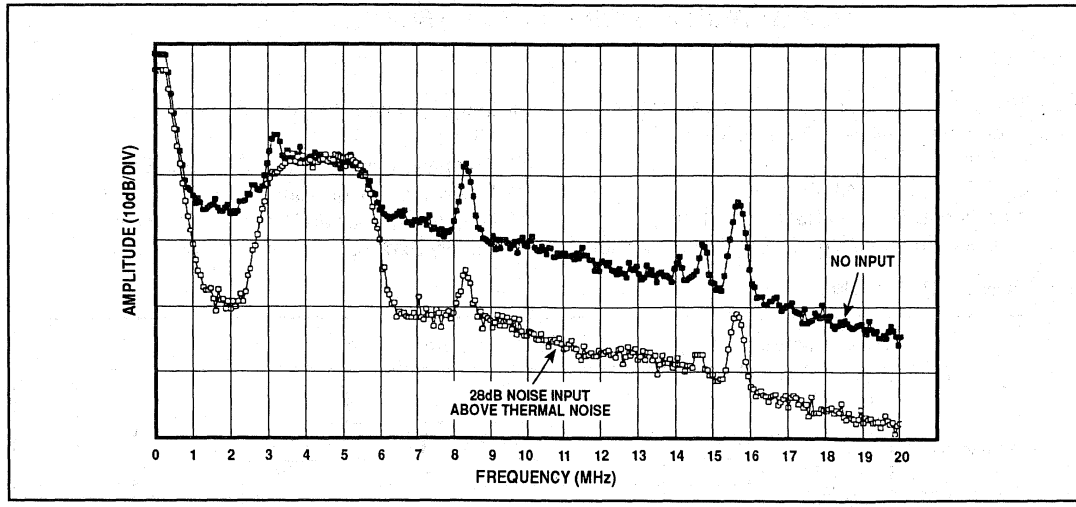


Fig. 5 GP2010 signal down-conversion AGC IF out

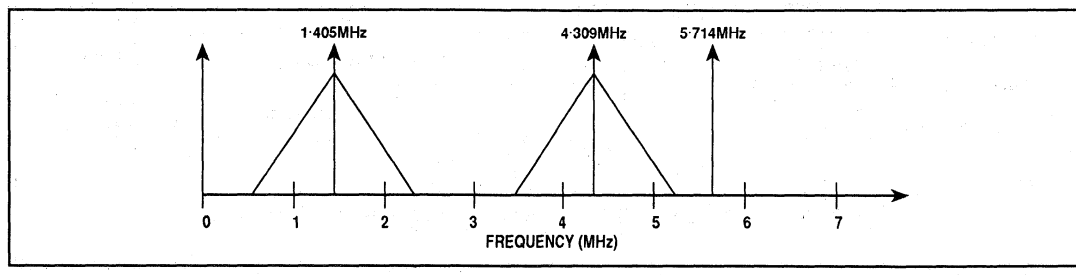


Fig. 6 GP2010 signal down-conversion sampling

Antenna and LNA Selection

The GP2010 has been designed to use the signal from a GPS antenna with a low noise amplifier (LNA) attached (an Active Antenna). The GP2010 performance cannot be guaranteed with a passive antenna. If the gain of the LNA is greater than approximately 10 (20dB), the noise figure of the complete receiver will then be dominated by the low LNA noise figure.

However, care should be taken to ensure that the gain of the LNA is high enough to allow the GP2010 to function correctly in a GPS receiver.

The document *GP2010 – design with the GP2010* (AN4364) refers, under *Antenna Details*, to a minimum required LNA gain of 16dB, including all the losses associated with RF filtering and coax cables, for the GP2010 to operate successfully. To a first approximation, the noise figure of the whole RF front end in a GPS receiver is:

$$NF = F_1 + \frac{(F_2 - 1)}{(G_1 - L_1)}$$

where F_1 = noise figure of Active Antenna LNA
F_2 = noise figure of GP2010
G_1 = RF gain of Active Antenna LNA
L_1 = loss due to RF filtering and cabling after LNA

The typical noise figure for the GP2010 is quoted as 9dB, while that for an LNA is 2·5dB and the typical gain for the Active Antenna is 26dB. The typical loss in a length of coax and associated RF filtering is variable; in the example below, a figure of 2dB has been used for a 2 metre length of cable.

Hence, the typical noise figure for the whole front end will be:

$$NF = 2{\cdot}5 + \frac{(9-1)}{(26-2)} = 2{\cdot}83\text{dB}$$

This shows that, in this case, the noise figure is dominated by that of the LNA.

GP2021 DIGITAL CORRELATOR ARCHITECTURE

FEATURES

- 12 Fully Independent Correlation Channels Configurable for either GPS or GLONASS Operation
- 1pps UTC Aligned Timing Circuit
- On-chip Dual UART and Real-time Clock
- Compatible with 16-bit and 32-bit Microprocessors
- Memory Control Logic for the ARM60 Microprocessor
- Compatible with GP2010 RF Front End
- Power Dissipation 150mW Typical
- Low Voltage/Current Power-down Mode
- Battery Back-up Voltage 2·2V (Minimum)

FUNCTIONAL OVERVIEW

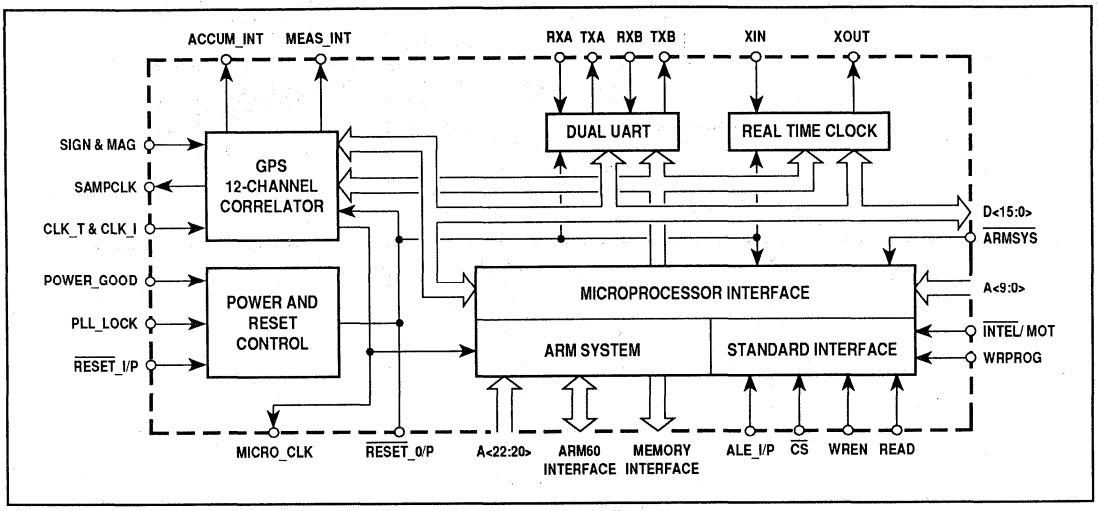


Fig. 7 GP2021 block diagram

The GP2021 (Fig. 7) can have all channels configured independently for either GPS or GLONASS satellites. Each channel can also be disabled for power saving purposes.

The GP2021 accepts 1-bit or 2-bit digital signals through one of two pairs of selectable inputs so that it can be used with up to two antennas. It can also be configured to accept input signals in real (both components in-phase) or complex (one component in-phase, the other component quadrature phase) form.

The GP2021 supplies two programmable interrupts for accessing the accumulation and measurement data.

The 40MHz clock required by the correlator chip can be derived from a GP2010 front end.

Microprocessor Interface

The GP2021 is compatible with 16- and 32-bit microprocessors. It supports four styles of microprocessor:

- ARM60
- Motorola
- Intel 80186
- Intel 486

In ARM60 mode, on-chip logic provides direct interfacing to the ARM60 microprocessor and the systems memory without any additional supporting hardware. For other microprocessors, additional external logic may be required.

Dual UART

There are two independent UARTs on the GP2021 which have programmable data rates, for both transmit and receive, between 300 and 76·8Kbaud. The parity bit can be programmed to be odd, even or none.

There are 8 byte deep FIFOs on both transmit and receive. The UARTs are accessed by polling

Real Time Clock

The real time clock (RTC) uses a 32kHz watch crystal and can be used to maintain a measure of elapsed time during GP2021 Power-down mode. This can be used to improve the TTFF by enabling prediction of satellite visibility and Doppler frequency offsets from the estimated receiver location.

Using a 24-bit 1-second counter, the RTC has a range of approximately 194 days.

The RTC Block also contains a Watchdog which causes a chip reset if it is not accessed for approximately 2 seconds. The Watchdog function can be disabled.

Power and Reset Control

The GP2021 has a Power-down mode which allows the supply voltage to drop to 2·2V (minimum). In this mode all GP2021 functions are disabled except for the RTC. During power-down the microprocessor clock is maintained to the end of the current clock cycle (falling edge) to prevent corruption of battery backed RAM, and all inputs (except those relevant to the Power and Reset Control block) are clamped to known logic levels to prevent power consumption by extraneous switching. There is no requirement for external pull-up or pull-down resistors. A GP2021 reset can also be initiated by use of the front end PLL lock indicator pin.

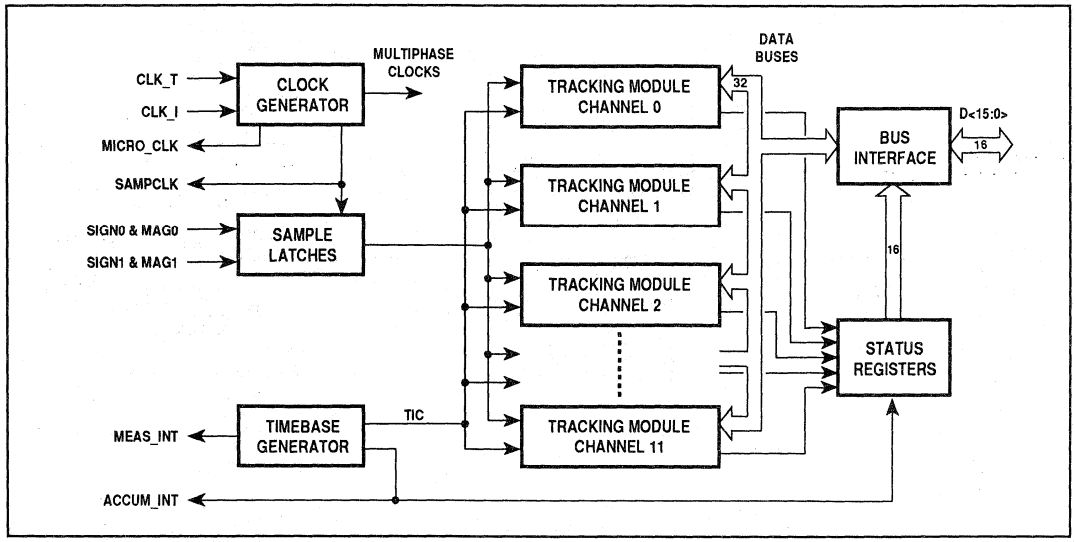


Fig. 8 GP2021 correlator block diagram

CORRELATOR DESCRIPTION

The GP2021 Correlator block is shown in Fig. 8; the constituent elements are described in the following sections.

Clock Generator

The Clock Generator accepts a differential input clock, CLK_T/CLK_I, normally at 40MHz. From this signal it generates:

(i) Multi-phase clocks for internal use by the rest of the device.
(ii) MICRO_CLK: a 20MHz clock provided as an output for the microprocessor.
(iii) SAMPCLK: a 5·714MHz clock for internal sampling of the input signal and also provided as an output for possible use by the front end as a sample clock.

Timebase Generator

The Timebase Generator generates:

(i) ACCUM_INT: a programmable interrupt which is normally used as a trigger to access new accumulation data from the tracking modules. The default interrupt period is 505·05μs for a master clock of 40MHz.
(ii) TIC: a signal of programmable period which is used to sample and latch the Tracking Modules measurement data – all at the same instant. The default TIC period is 0·0999999 seconds for a master clock of 40MHz.
(iii) MEAS_INT: an interrupt generated from TIC which is normally used to access new measurement data from the measurement data registers or as a timebase for switching software module tasks.

Sample Latches

The input signals at SIGN0, MAG0, SIGN1 and MAG1 are sampled (normally at 5·714 MHz) and latched for distribution to the Tracking Modules.

Bus Interface

The Bus Interface controls data transfer between the external 16-bit and the internal 32-bit data bus.

Status Registers

This block consists of four registers, three registers containing status information relevant to the accumulation data and one register relevant to the measurement data.

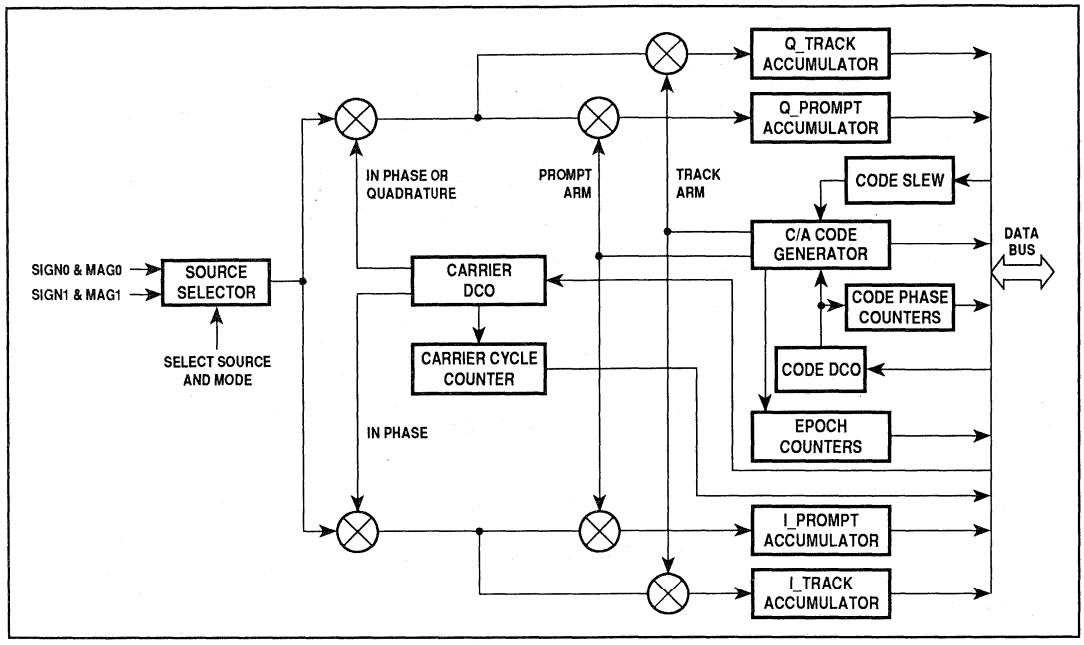


Fig. 9 GP2021 tracking module architecture

Tracking Module

The GP2021 has 12 identical tracking module blocks, one for each channel. Each block (shown in Fig. 9) contains all the components necessary for acquiring and tracking the received signal (code generator, code DCO, carrier DCO, mixers and accumulators). Each block also contains other functional blocks which are used to produce part of the measurement data set (epoch counter and carrier cycle counter).

Code Generator

The Code Generator can generate the following pseudo-random codes:

(i) GPS satellite C/A codes for PRNs 1 to 32.
(ii) Pseudolite C/A codes for PRNs 33 to 37.
(iii) INMARSAT GIC codes for PRNs 201 to 211
(iv) GLONASS C/A code.

The generated code is supplied to the Prompt and Track arms. The Track arm code can be configured to 4 different modes with respect to the Prompt arm code phase:

(i) Early: permanently 1/2 chip early (advanced).
(ii) Late: permanently 1/2 chip late (retarded).
(iii) Early-Minus-Late: signed difference of Early and Late.
(iv) Dithered: alternates between Early and Late every 20ms.

Code DCO

The Code DCO clocks the code generator at nominally twice the C/A code rate (2·046MHz). This rate is required to produce the Track arm codes phased by 1/2 chip with respect to the Prompt arm code.

A 26-bit long counter clocked at 40/7MHz (for a 40MHz master clock) provides a resolution of approximately 85·149mHz (42·575mHz at the C/A code rate).

It is programmed via the following registers:
CHx_CODE_DCO_INCR_HIGH: DCO bits 24 to16 and
CHx_CODE_DCO_INCR_LOW: DCO bits 15 to 0.

A control word of $016EA4A9_{hex}$ gives a C/A code rate of nominally 1·023 MHz.

Code Phase Counters

This block contains counters for determining the code phase of the Prompt arm. At each TIC the counters are sampled and the data is stored in the following registers:

CHx_CODE_PHASE: gives the number of 1/2 chips of code phase in the range 0 to 2046.

CHx_CODE_DCO_PHASE: gives the fractional code phase below 1/2 a chip. It takes values from 0 to 1023 with a resolution of 1/2048 (approximately 0·5 ns or 0·15 m) of a chip.

Epoch Counters

This block contains counters for determining the complete number of code cycles (epochs) on the Prompt arm. At each TIC, the counters are sampled and the data is stored in the CHx_EPOCH_COUNT register, which contains the number of 1 ms (in the range 0 to 19) and 20ms (in the range 0 to 49) epochs. Hence, the Code Phase registers can be combined with the Epoch Count register to give a code time between 0 and 1 second at a resolution of approximately 0·5ns.

Carrier DCO

The carrier DCOs are used to mix the input signal to baseband prior to correlation with the locally generated codes.

A 27-bit long counter clocked at 40/7MHz (for a 40MHz master clock) provides a resolution of approximately 42·575mHz.

The carrier DCOs generate 4 level, 8 phase sinusoids with the sequence over 1 cycle as shown in Fig. 10.

When the input signal is already in complex (I, Q) form the quadrature DCO can be configured to generate an in-phase carrier.

It is programmed via the following two registers:

(i) CHx_CARRIER_DCO_INCR_HIGH: DCO bits 25 to 16.
(ii) CHx_ CARRIER_DCO_INCR_LOW: DCO bits 15 to 0.

When used with a GP2010 a control word $01F7B1B9_{hex}$ gives a carrier DCO frequency rate of approximately 1·405397 MHz.

Carrier Cycle Counter

This block contains counters for determining the number (whole and fractional) of in-phase carrier DCO cycles between the last 2 TICs.

CHx_CARRIER_CYCLE_COUNTER_HIGH and CHx_CARRIER_CYCLE_COUNTER_LOW:

The block provides the number of positive going zero crossings of the in-phase carrier DCO between the last 2 TICs. The counter is 20 bits long.

CHx_CARRIER_DCO_PHASE: gives the in-phase carrier DCO fractional carrier phase sampled at the current TIC. The counter is 10 bits long to give a resolution of 1/1024 (approximately 0·2 mm at L1) of a cycle.

The above registers are used to form the integrated carrier phase measurements.

Accumulators

Four 16-bit accumulators contain the results of the code correlation over the code period of nominally 1ms. This data can be accessed through the following registers:

(i) CHx_I_TRACK: The accumulation from the in-phase Track arm.
(ii) CHx_Q_TRACK: The accumulation from the quadrature Track arm.
(iii) CHx_I_PROMPT: The accumulation from the in-phase Prompt arm.
(iv) CHx_Q_PROMPT: The accumulation from the quadrature Prompt arm.

Status Registers

There are 4 status registers, three associated with the accumulators and one with the measurement data:

(i) ACCUM_STATUS_ A: Amongst other things, this register contains a status bit for each channel which is set when new accumulation data is available for that channel.
(ii) ACCUM_STATUS_B: Amongst other things, this register contains a status bit for each channel which is set when new accumulation data becomes available for that channel before the last accumulation result was read. This gives an indication that the processor is not accessing some or all of the accumulation registers at a fast enough rate.
(iii) ACCUM_STATUS_C: This register contains a status bit for each channel which is set or cleared according to whether the Track arm of that channel is generating Early or Late code when the arm is configured in Dither mode.
(iv) MEAS_STATUS_A: Amongst other things, this register contains a status bit for each channel which is set when new measurement data becomes available for that channel before the last measurement data was read. This gives an indication that the processor is not accessing some or all of the measurement data registers at a fast enough rate.

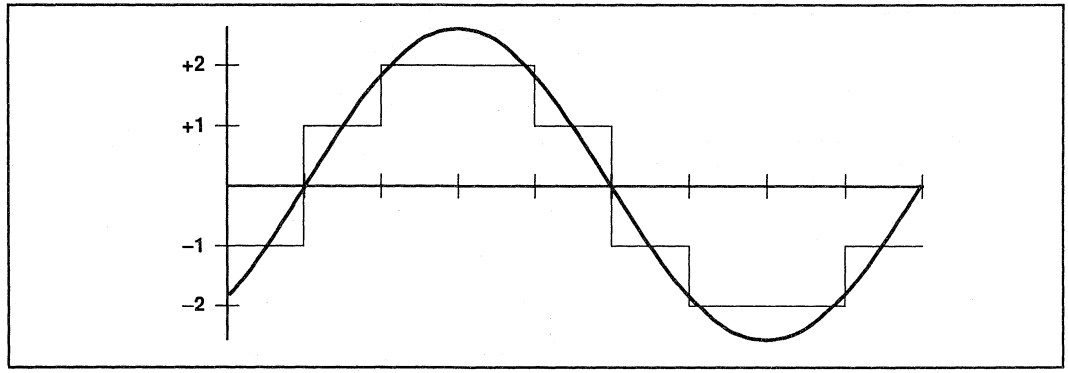


Fig. 10 GP2021 carrier DCO

GPS BUILDER-2 HARDWARE AND SOFTWARE OVERVIEW

SYSTEM OVERVIEW

GPS Builder-2 is a development system which assists in the design and development of a GPS Receiver. This section provides an overview of the component parts of GPS Builder-2. The main elements are:

- Mother board
- Daughter board
- Software

The GPS Builder-2 hardware (Fig. 11) consists of a mother board, a daughter board and an active antenna.

The mother board (Fig. 12) is a standard PC card which fits into an ISA bus slot. The daughter board (Fig.13) contains the GP2000 chipset and is effectively the core of a GPS receiver. It can be detached from the mother board if required. There is space for a second front end GP2010 circuit to be added.

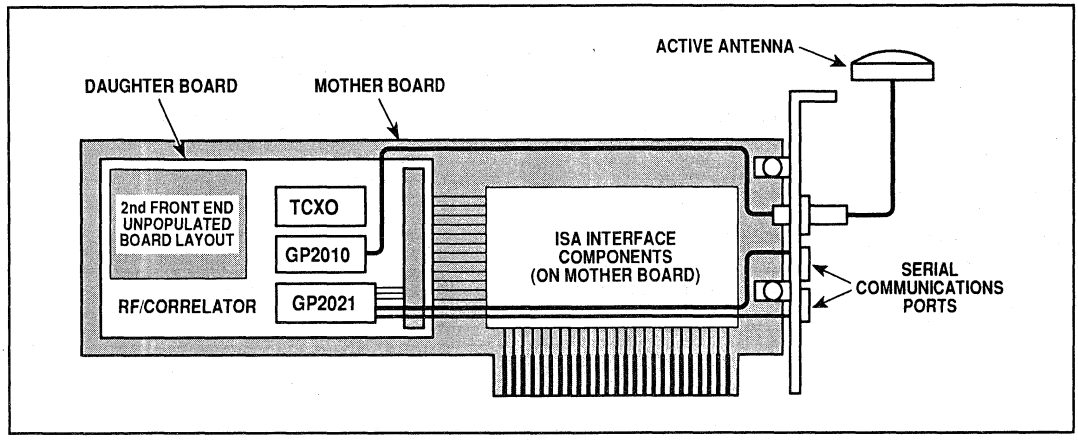


Fig. 11 GPS Builder-2 hardware (simplified)

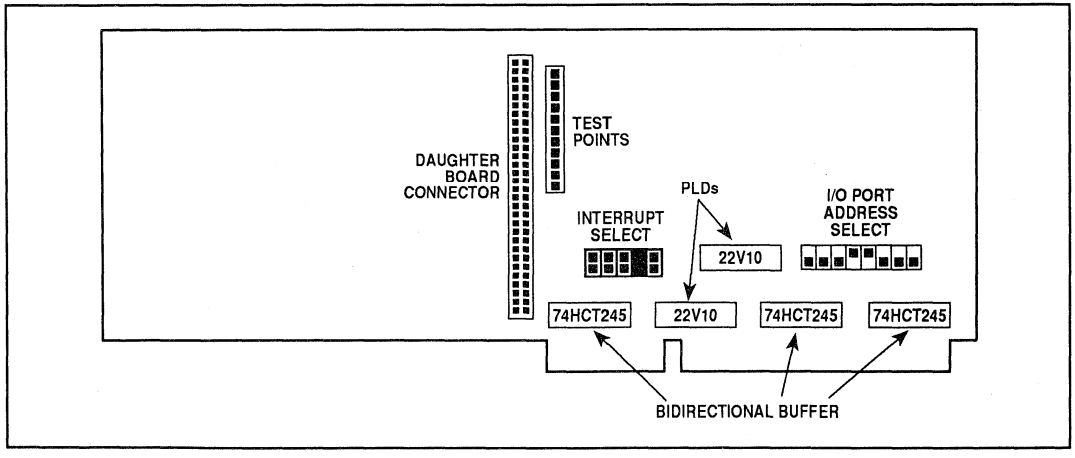


Fig. 12 GPS Builder-2 mother board

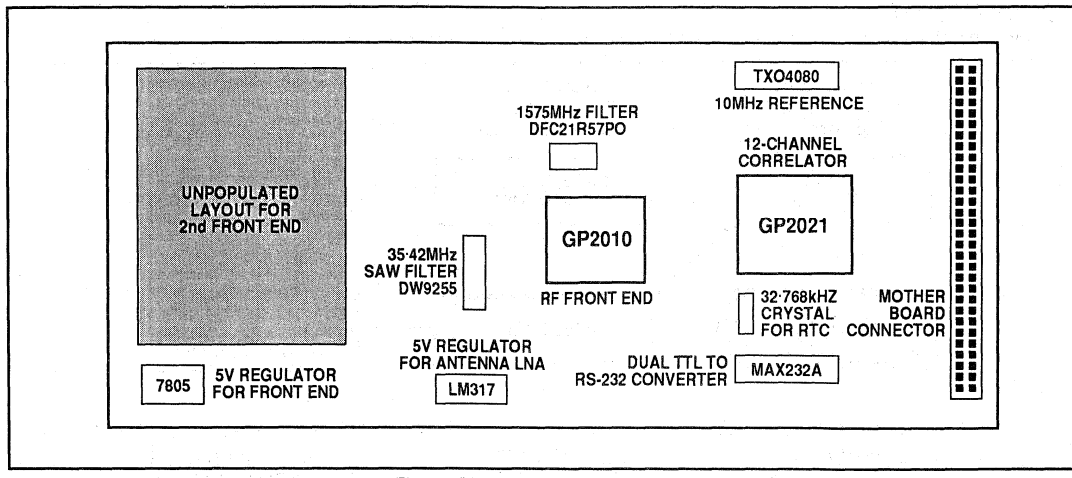


Fig. 13 GPS Builder-2 daughter board

Address and Interrupt Settings

To remove possible conflicts with other hardware in the host PC, the GPS Builder-2 can be configured to use one of 16 I/O port addresses (Table 1) and one of 5 interrupts (Table 2).

I/O port address (Hex)	Common assignment
200-21F	Game controller adaptor
220-23F	
240-25F	
260-27F	LPT3 adaptor
280-29F	
2A0-2BF	
2C0-2DF	
2E0-2FF	COM2 adaptor
300-31F	
320-33F	HDD controller
340-35F	
360-37F	PC Network & LPT2 adaptor
380-39F	
3A0-3BF	Monochrome display & LPT1 adaptor
3C0-3DF	CGA, MCGA, EGA and VGA adaptor
3E0-3FF	FDD controller & COM1 adaptor

Table 1 GPS Builder-2 address settings

Interrupt number	Common assignment
10	Unassigned
11	Unassigned
12	Unassigned
14	HDD controller
15	Unassigned

Table 2 GPS Builder-2 interrupt settings

SOFTWARE OVERVIEW

An overview of the software is shown in Fig. 14. It includes start-up files and log files.

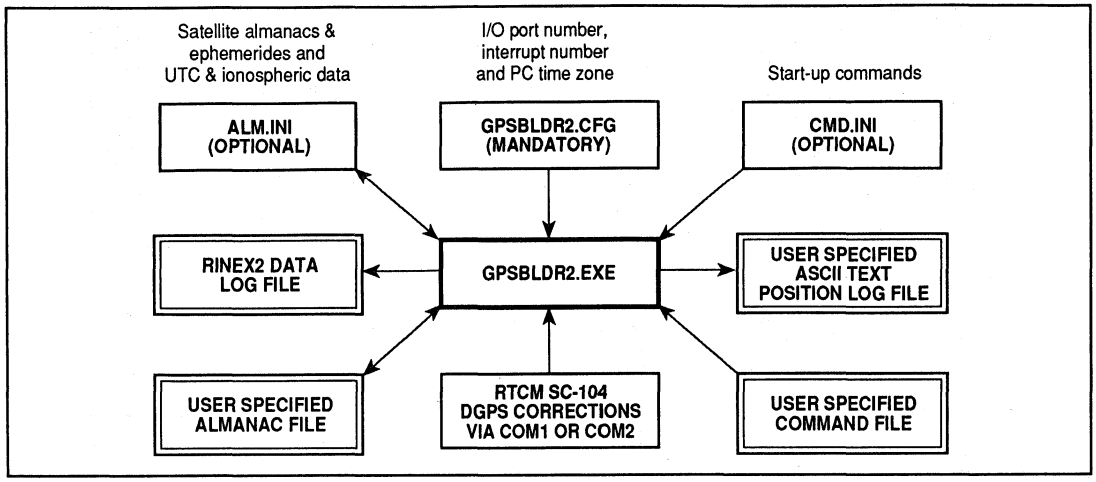


Fig. 14 Software overview

GPSBLDR2.CFG

GPSBLDR2.CFG is a mandatory file, containing user settings of the GPS Builder-2 board I/O port number, interrupt number and the time zone offset (hours) of the host PC clock.

Example file

```
300 Hexadecimal I/O port address for GPS Builder-2 card
11  Decimal interrupt level for GPS Builder-2 card
0   Time zone
```

CMD.INI

CMD.INI is an optional default command file loaded at program start-up. It contains a series of GPS Builder-2 commands to be executed at program start-up. User-specified command files can also be executed during the program operation using the *CF <filename>* command.

Example file

```
IP  N51  34·34 W001  48·55  161
RP  N51  34·34 W001  48·55  161
CH  12
EM  5·0
GM  10·0
```

ALM.INI

ALM.INI is an optional default almanac file loaded at program start-up. It is a binary file which contains almanacs and ephemerides for all satellites and data for the ionospheric model and the GPS System time to UTC correction polynomial.

The almanac file, ALM.INI, can be updated at program exit using the *QA* command, or to a user specified file using the *SA <filename>* command. A user specified almanac file can be read during program execution with the *RA <filename>* command.

ASCII Text Log File

ASCII Text Log File saves data in comma delimited fields containing data such as date, time, longitude, latitude, height, speed, heading, channel activity (satellite allocated and lock status) etc.

RINEX2 File

The RINEX2 File saves data in RINEX2 (Receiver Independent Exchange format) Observation (pseudo-range (m), Doppler (Hz), carrier phase (cycles)) and Navigation (ephemeris) files.

Software Attributes

500 Kbytes of 'C' source code
100 Kbytes of 'H' include files
167 Kbytes executable *
260 Kbytes of free base memory required *
Compiles with Borland™ C/C++ V3.1 and V4.0 **
Compiles to either 16- or 32-bit instruction set
Some in-line assembler and compiler-specific code

* 4.0/ 32-bit compilation
** Also V4.5 but not fully evaluated

Concurrent Tasks

The software performs the following concurrent tasks:

Read the accumulators
Control the tracking loops
Monitor the loop lock conditions
Update receiver position/velocity estimates
Parse the satellite data message
Collect measurement blocks
Satellite ephemeris calculations
Control satellite selection strategy
Serial communications interrupt routines

Multi-Tasking (Fig. 15)

The concurrency necessary in the software is controlled by a simple multi-tasking operation system:

Procedures are either interrupt driven or tasks.
Only one task can be active at any time.
Task activation is managed via the primary interrupt routine.

Task Management

Tasks can be either active or suspended. Only one task is active at a time. Tasks suspend themselves upon partial or full completion.

Task activation occurs at the end of the suspension interval or by direct activation. Suspension intervals are multiples of approximately 0·1 seconds.

Task priority determines which Task gets the processor during Task conflict. Main() is always the lowest priority Task.

Processor retention can be achieved by disabling Task switching or by disabling interrupts.

All Tasks have separate stacks for context retention.

Data Structures

Global data structures exist to share data between concurrent parts of the software (Tasks and interrupt routines). Data can be associated to 3 basic areas:

(i) Channel related (e.g. accumulation data, tracking loop states etc.).
(ii) Satellite related (e.g. ephemeris data, almanac data etc.).
(iii) Receiver related (e.g. pos/vel vector, clock model etc.).

The main data structures in GPS Builder-2 are:

(i) Channel structure (15840 bytes for 12 channels).
(ii) Observation data (10440 bytes for 30 measurement blocks).
(iii) Ephemeris data (6720 bytes for 32 satellites).
(iv) Almanac data (1472 bytes for 32 satellites).

Other data areas include:

(i) ISR stack (3096 bytes [3×1032 for a re-entry level of 3]).
(ii) Task local stack (20000 bytes total for 5 tasks).

Data Access

Indivisible access is required to shared variables and data structures.

Protected regions of code (regions where Task switching is inhibited) are created by using the PROTECT variable.

A non-zero value of PROTECT prevents Task switching by the interrupt routine. Enclosing protected code by the statements PROTECT++ and PROTECT-- allows nested regions of protected code to be created.

```
PROTECT++; /* Get a local copy of the
navigation state. */
CurrentNavState = NavState; PROTECT--;
```

Disabling interrupts allows indivisible access to global variables manipulated in the interrupt service routine.

Neither Task switching nor interrupts should be disabled for more than a few microseconds to ensure normal software operation.

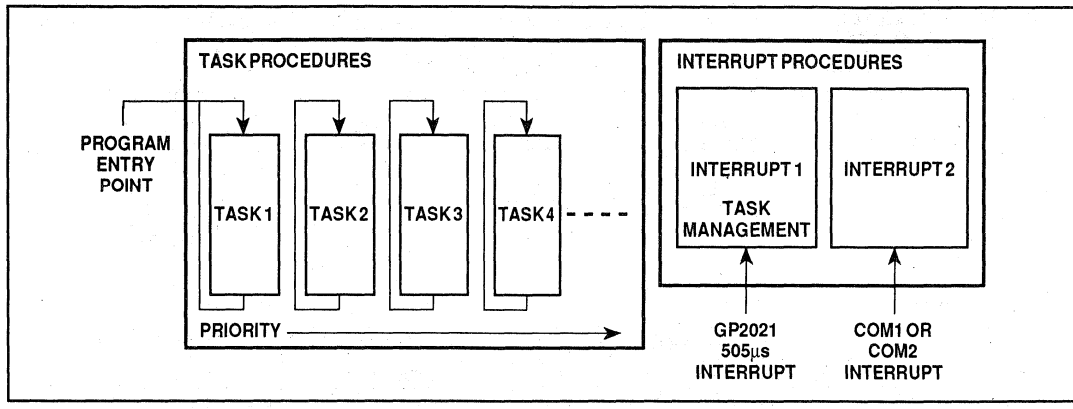


Fig. 15 Multi-tasking

Software Structure (Fig. 16)

GPS Builder-2 consists of two interrupt routines and five Tasks.

The interrupt routines are:

(i) GPISR: Correlator Interrupt Service Routine (interrupts approximately every 505µs).

(ii) NewSerialInt: Serial port interrupt service routine (for DGPS correction data).

The Tasks (in increasing order or priority) are:

(i) Main: Initialisation, satellite visibility predictions, allocation of satellites to channels, navigation solution and position update.

(ii) TProcSbf: Parse and update satellite subframe data message.

(iii) TRTCM: Parse and update RTCM SC-104 DGPS data.

(iv) TDisplay: Update the display.

(v) TBeep: Sound the PC speaker (template for new Task).

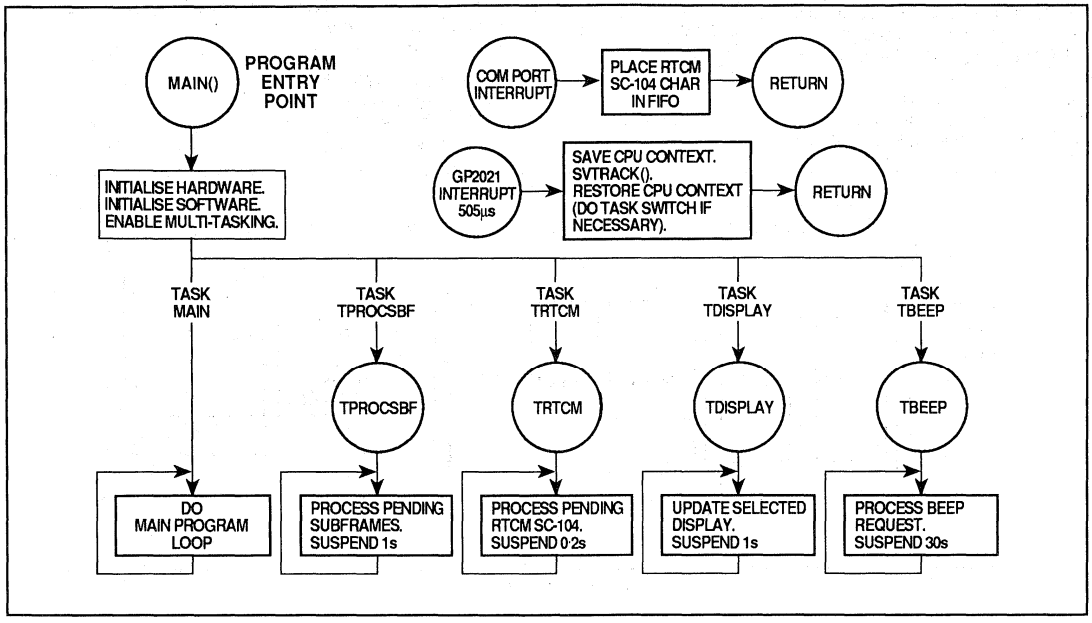


Fig. 16 Software structure

SVTRACK() (Fig. 17)

SVTRACK() is composed of 3 isolated tasks:

(i) BufferAccum Phase: For each active channel, if new accumulation data is available (approximately every 1ms), read and store the data in the accumulations buffer. Perform carrier acquisition and tracking, and manipulate the channel epoch counters if necessary.

(ii) TakeMeas Phase: At every TIC (approximately every 0·1s) for all active channels read and store the measurement data (code phase, carrier phase, carrier cycle count and epoch counters) into the observation buffer (for use by the navigator function).

(iii) ProcAccum Phase: If available, process the buffered accumulation data. Perform code acquisition and tracking. Perform data bit and frame sync. Emit the satellite data subframes to TProcSbf() for processing.

SVTRACK() Re-Entrancy (Figs. 18, 19 and 20)

For 12 active channels, SVTrack() cannot always complete within 1 interrupt period (505μs) Hence, the lower rate tasks – TakeMeas and ProcAccum – are made re-entrant.

Re-entrancy into the interrupt service routine is possible up to a nesting level of 3.

Upon entry to SVTrack() interrupts are disabled. BufferAccum is non re-entrant and must complete before the next interrupt

Both TakeMeas and ProcAccum are interruptable.

If either TakeMeas or ProcAccum is not in progress (from a higher nesting level) once BufferAccum has completed then the appropriate phase (TakeMeas or ProcAccum) will be started.

Software Porting Issues

It is likely that all GPS receiver software will contain some host or implementation dependent features. GPS Builder-2 software is no exception. However, to facilitate the porting of GPS Builder-2 code to different processors, such features are kept to a minimum by maximising the use of a high-level programming language ('C') and grouping unavoidable dependencies in single modules.

As a consequence of this, and the desire to maintain a high level of generality, scope exists for improvement to the general efficiency and reduction in processor loading of the software. This can be achieved by optimising the software for a particular system (processor, memory structure etc.), although at the expense of further portability.

Within GPS Builder-2 the host dependencies are basically hardware related (PC and processor) or software related (Borland™ C/C++, DOS and 80x86 assembly language).

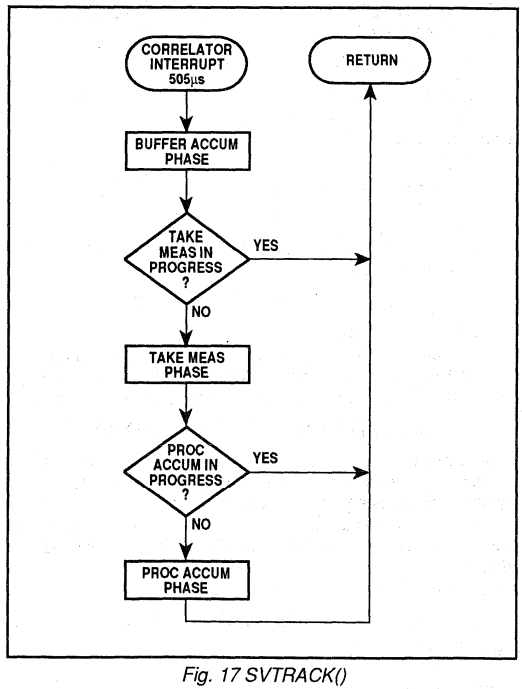


Fig. 17 SVTRACK()

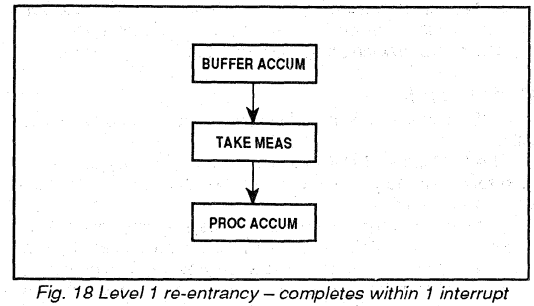


Fig. 18 Level 1 re-entrancy – completes within 1 interrupt period

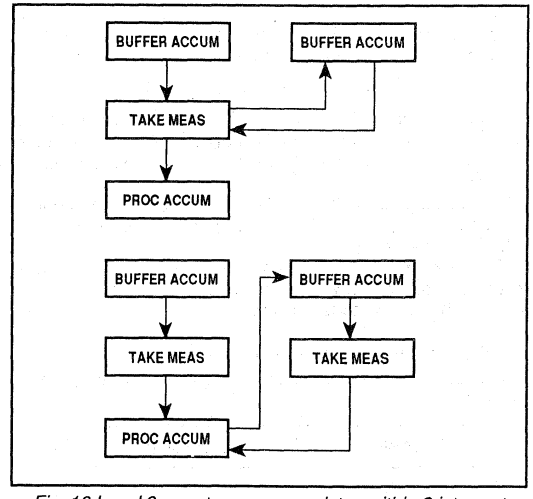


Fig. 19 Level 2 re-entrancy – completes within 2 interrupt periods

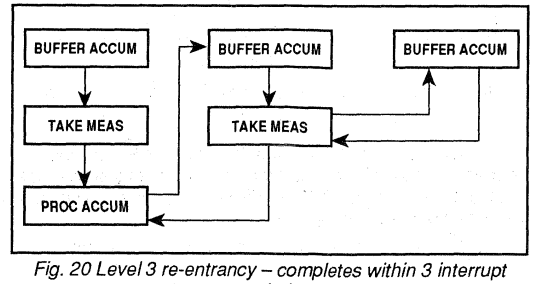


Fig. 20 Level 3 re-entrancy – completes within 3 interrupt periods

GPS BUILDER-2 SIGNAL PROCESSING ALGORITHMS

CODE ACQUISITION AND TRACKING

For signal acquisition to occur, both the GP2021 code phase and carrier frequency must match the incoming code phase and carrier frequency to such an extent that the resultant correlation is above the detection threshold.

GPS Builder-2 performs a search in the code phase/carrier frequency plane by searching across all code phases at a series of frequency bins until the signal is detected.

Once signal detection occurs, the code and carrier tracking loops are closed.

Code tracking is achieved using a Phase Locked Loop. Carrier tracking is achieved using a Frequency Locked Loop.

The carrier tracking loop aids the code tracking loop.

Code Search

GPS Builder-2 uses a sliding-replica search for code acquisition.

The GP2021 code DCO is programmed to a slightly higher chip rate than the predicted rate so that the codes 'slide' past each other with time.

The default programmed offset gives a search rate of 0·25 chips per millisecond. Hence, a complete code search (1023 chips) at a given frequency takes about 4 seconds to complete.

The frequency bins are 500Hz wide. Therefore, to search a frequency space of ±10·25kHz takes about 164 seconds to complete.

Code Lock

The current correlation power is given by the sum of the squares of the in-phase and quadrature accumulations.

$$\text{Correlation power} = (I^2+Q^2)$$

When the instantaneous value of (I^2+Q^2) exceeds a fixed threshold above the noise floor, signal detection is declared. A filtered version of (I^2+Q^2) is then monitored for continued code lock.

The accumulator noise floor is determined from the product of the samples from the GP2010 output with the output from GP2021 carrier DCOs.

The effect of code phase error and carrier frequency error on the correlation power level has to be included in the determination of the code lock threshold.

Code Lock Indicator - Noise Floor

The GP2010 has the distribution at its output as given in Table 3:

Level	Percentage of time
+3	15
+1	35
−1	35
−3	15

Table 3

The carrier DCOs have the following distribution over 1 cycle:

+2 +2 +1 −1 −2 −2 −1 +1

The noise floor for one accumulator (I^2+Q^2) is given by the mean square of the product of the above two sequences (taking into account the GP2010 distribution) times the number of samples over one millisecond.

$$(I^2+Q^2) = (22{\cdot}5\times0{\cdot}3+2{\cdot}5\times0{\cdot}7)\times40/7\times1000 = 48{,}571$$

Therefore, the noise floor,

$$(I^2+Q^2) = 2\times48,\ 751 = 97,\ 142$$

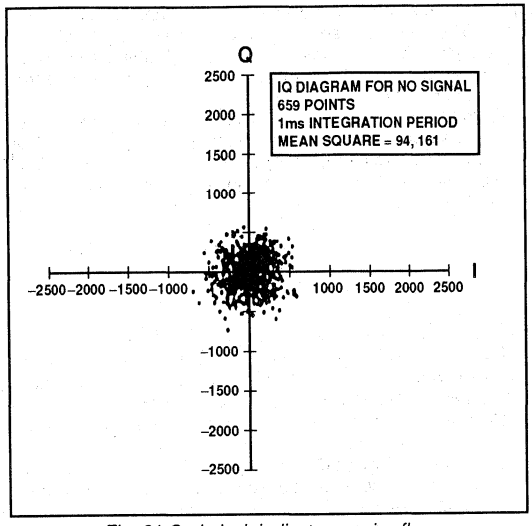


Fig. 21 Code lock indicator – noise floor

Code Lock Indicator Acquisition Threshold

The noise floor with no signal present is 97,142. For reliable acquisition, the minimum post-detection SNR will be about 6dB. This corresponds to an acquisition threshold, T_A, of:

$$T_A = 97{,}142\times10^{0{\cdot}6} = 386{,}729$$

The correlation power degrades as a function of a code phase error, ΔC chips, by:

$$\text{Correlation loss} = 20\log(1-\Delta c)$$

Therefore, for $\Delta c = 0{\cdot}25$ chips, correlation loss = 2·5dB.

The correlation power degrades as a function of a carrier frequency error, Δf Hz, by:

$$\text{Correlation loss} = 20\log\left(\frac{\sin(\pi\Delta fT)}{\pi\Delta fT}\right)$$

Therefore, for $\Delta f = 250$Hz (500Hz/2), correlation loss = 0·9dB Therefore, including the above losses,

$$T_A = 97{,}142\times10^{0{\cdot}26} = 176{,}769$$

Code Tracking Loop

GPS Builder-2 uses an Early-Minus-Late discriminator for code tracking. The Track arm of the correlator is set 1/2 chip early of the Prompt arm. The code phase error is then given by:

$$EML = (IT^2+QT^2)-(IP^2+QP^2)$$

i.e., when the loop is locked the Track arm will be nominally 1/4 chip early and the Prompt arm 1/4 chip late of the actual, but physically non-existent, prompt or on-time code.

The code tracking loop uses a second order Phase Locked Loop. (Note: this can be a first order PLL when used with carrier aiding).

The open-loop transfer function is:

$$Y(s)/X(s) = G(s) = (T_2s+1)/T_1s$$

where $T_1 > T_2 > 0$

or, rearranging:

$$T_1s\times Y(s) = (T_2s+1)\times X(s)$$

Expressing this in the time domain gives:

$$T_1 \times \frac{dy}{dt} = T_2 \times \frac{dx}{dt} + x$$

Over a sample interval ΔT:

$$\frac{dy}{dt} = \frac{(y_i - y_{i-1})}{\Delta T}; \quad \frac{dx}{dt} = \frac{(x_i - x_{i-1})}{\Delta T}$$

therefore:

$$T_1 \times (y_i - y_{i-1}) = T_2 \times (x_i - x_{i-1}) + X_i \Delta T$$

or more conveniently:

$$y_i = y_{i-1} + \left(\frac{T_2}{T_1}\right) \times (x_i - x_{i-1}) + \left(\frac{\Delta T}{T_1}\right) \times x_i$$

The loop is designed so that the factors (T_2/T_1) and $(\Delta T/T_1)$ are powers of 2 to reduce processor loading.
T_1 and T_2 are related to the loop characteristics as follows:

Loop natural frequency, $\omega_n = \sqrt{\frac{K_\phi \times K_0}{T_1}}$

Damping factor, $\zeta = \left(\frac{T_2}{2}\right)\omega_n$

Pull-in range $\Delta\omega_p = \frac{4\sqrt{2\zeta\omega_n K_\phi K_0 - \omega_n^2}}{\pi}$

Pull-in time from $\Delta\omega_0$, $T_p = \frac{\pi^2}{16} \times \frac{\Delta\omega_0^2}{\zeta\omega_n^3}$

Pull-out range, $\Delta\omega_{p0} = 1{\cdot}8 \times \omega_n \times (\zeta + 1)$

Closed loop bandwidth, $W = \omega_n\left(\frac{1+4\zeta^2}{8\zeta}\right)$ Hz

K_ϕ and K_0 are the phase error detector gain (the EML discriminator gain, units per radian of code phase error) and the code DCO conversion gain (rad/s per control unit) respectively.

Carrier Acquisition & Tracking

Carrier Tracking Loop

The carrier tracking loop tracks the incoming carrier to produce carrier cycle and carrier phase measurements to smooth the code pseudo-ranges. It also aids the code tracking loop since the ratio of the code to carrier frequency is a constant. Carrier acquisition and tracking is initially achieved using a 4-quadrant frequency discriminator to reduce the frequency error from a few hundred Hertz to a few Hertz.

This is followed by a 2nd order Frequency-Locked Loop (FLL) which has zero steady-state error for a constant rate of change in frequency (acceleration).

FLLs offer superior dynamic performance, robustness and insensitivity to interference over PLLs.

Four-Quadrant Frequency Discriminator

The discriminator correction term is derived by comparing I and Q correlations between successive readings (assuming a data bit transition has not occurred):

$$\Delta I = I_k - I_{k-1}$$
$$\Delta Q = Q_k - Q_{k-1}$$

The choice of correction and sign of application is determined from the current correlations and their respective magnitudes (see Fig. 22).

For $|I_k| > |Q_k|$: IF $I_k > 0$ correction $= \Delta Q$, ELSE correction $= -\Delta Q$
For $|I_k| \leq |Q_k|$: IF $Q_k > 0$ correction $= -\Delta I$, ELSE correction $= \Delta I$

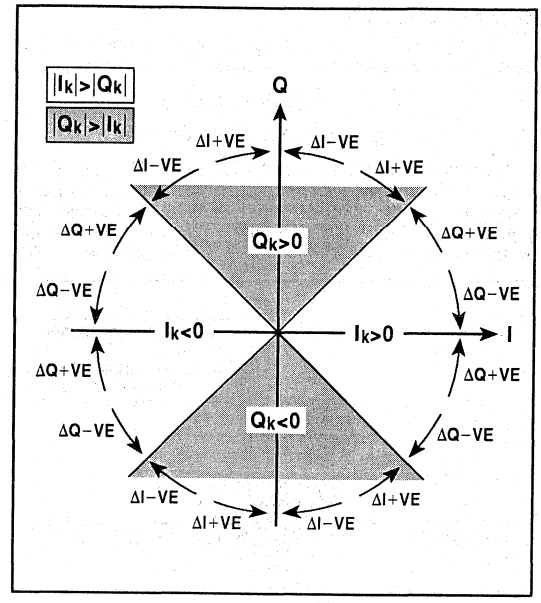


Fig. 22 Four-quadrant frequency discriminator

Frequency-Locked Loop

The discriminator correction term is derived by comparing I and Q correlations between successive readings (assuming a data bit transition has not occurred) using the cross product:

$$f_k = Q_k I_{k-1} - I_k Q_{k-1}$$

For $I_k^2 + Q_k^2 \approx I_{k-1}^2 + Q_{k-1}^2$:

$$f_k = (I_k^2 + Q_k^2)\sin(\phi_k - \phi_{k-1})$$

where ϕ_k and ϕ_{k-1} are the carrier phases at successive readings.
Therefore, for small $\phi_k - \phi_{k-1}$,

$$f_k \approx (I_k^2 + Q_k^2)\Delta\phi,$$

where $\Delta\phi$ is the carrier phase change over 1 millisecond.

Using a discretised second order Jaffe-Rechtin filter of bandwidth B_{LF}, and normalising to the correlation power, the following frequency correction terms can be derived for the estimated carrier frequency:

$$\Delta\omega = \omega_k - \omega_{k-1} = T\dot{\omega}_k + \sqrt{2\omega_{nF} f_k}$$
$$\omega_{nF} = 1{\cdot}89 B_{LF}$$
T = sampling interval of 1ms.

The optimum setting for B_{LF} for a given rate of change of acceleration (jerk) is given by:

$$\frac{\ddot{\omega}}{\omega_{nF}^2} = \frac{0{\cdot}25}{T}$$

Carrier Lock Indicator

Carrier lock can be monitored by averaging the dot product between correlations:

$$\text{Lock indicator} = I_k I_{k-1} + Q_k Q_{k-1}$$

This quantity averages to zero until the loop locks which in turn drives the cross product, $Q_k I_{k-1} - I_k Q_{k-1}$, to zero. Once locked, the average value of the dot product can be used to estimate the signal power.

Data Demodulation

For coherent data demodulation the carrier samples are rotated through the average carrier phase, ϕ_K, as follows:

$$I_{new} = I_k\cos\phi_k + Q_k\sin\phi_k$$
$$Q_{new} = Q_k\cos\phi_k + I_k\sin\phi_k$$

I_{new} can be integrated over the bit period (20ms) to give a representation of the current data bit. To minimise computational loading the functions sin() and cos() are determined through look-up tables. Successful (no parity errors) data demodulation occurs for post-correlation SNRs down to approximately 5-6dB.

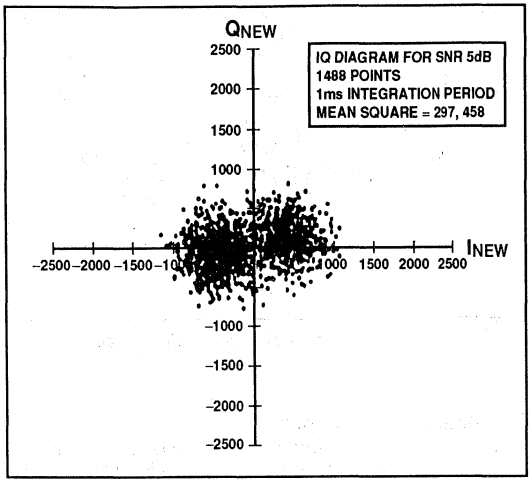


Fig. 23 Data demodulation with SNR = 5dB

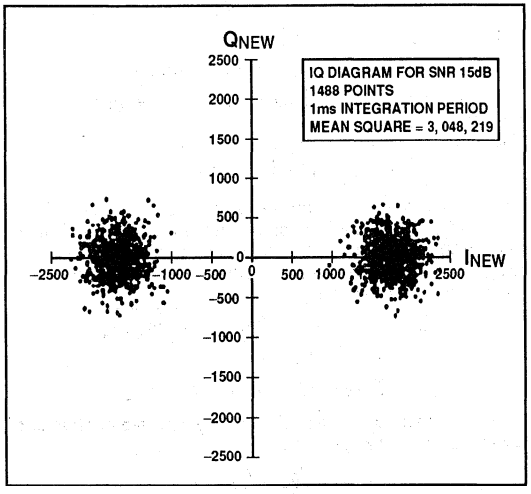


Fig. 24 Data demodulation with SNR = 15dB

Data Bit And Data Frame Synchronisation

Data Bit Synchronisation

The data bit transition is determined by performing a running sum of the in-phase correlations over a bit period at each of the possible twenty 1-millisecond epoch settings. The epoch with the largest integration is declared as the provisional data bit transition. If the best epoch does not change over a 2-second period then bit sync is declared at this position.

The 1ms Epoch Counter is slewed so that its value is zero at the data bit transition, if this is not already the case. The data bit transition position is continually monitored.

Data Frame Synchronisation

Frame sync is achieved by searching for the following parameters contained in the TLM and HOW words across 60 successive data bits (2 words):

(i) TLM preamble (10001011)
(ii) HOW subframe ID (1 to 5)
(iii) HOW zero bits (bits 29 and 30)

If all the above data is found, and the 2 words pass the parity check, then the value of the 20ms Epoch counter is checked. The 20ms Epoch Counter should have a value of zero at the start of each subframe and so a value of 10 at the end of the second word (HOW word). If its value is 10, then frame sync is declared. If it is not 10, then the 20ms Epoch Counter is slewed to its correct value.

Frame sync will then be declared 1 subframe later.

Observation Measurement Block

Measurement Blocks

At each TIC the following data is stored, for each active channel, to be used in the navigator function:

(i) If the channel has valid data
(ii) The satellite PRN assigned to the channel
(iii) The epoch count register (1ms & 20ms epoch counts)
(iv) The code phase register (number of 1/2 chips of code)
(v) The code DCO phase register (the fractional code phase)
(vi) The carrier DCO phase register (the fractional carrier phase)
(vii) The carrier DCO phase register at the last TIC
(viii) The carrier cycle count (whole cycles between TICs)
(ix) The lost lock indicator

Formulation of The Pseudo-Range, Pseudo-Range Rate and Integrated Carrier Phase

Formulation of The Pseudo-Range

At each TIC the pseudo-range is given by the time of reception of the signal minus the time of transmission. This measurement will include the receiver clock bias. Other corrections fo the satellite clock error, Earth rotation plus atmospheric and relativistic effects are applied later.

The time of transmission (modulo 1 second) is determined from the epoch counters and code DCO setting:

Transmit Time = 20×20ms_EPOCH_ COUNT
+1_ms_EPOCH_COUNT
+CODE_DCO_PHASE
−1/4 chip

The code DCO phase includes the number of 1/2 chips plus the fractional phase.

The 1/4 chip term is included because the measurement block data is referenced to the Prompt arm which is set 1/4 chip late in the EML Tracker.

The Reception Time is the receiver clock estimate of GPS System Time at the measurement block TIC. The receiver clock is assumed to be accurate to ±1/2 second to avoid any ambiguity in the pseudo-range. For all practical systems this will be the case.

Hence, Pseudo-range = Reception Time−Transmission Time (modulo 0·5 seconds).

The pseudo-range is transformed into units of metres.

The pseudo-range rate (including satellite and receiver clock drifts) can be determined from the offset of the carrier DCO from its nominal value:

$$\text{Pseudo-range rate} = -\Delta D \times c/L_1$$

where ΔD is the carrier DCO offset from its nominal value, c is the speed of light and L_1 is 1575·42MHz.

The nominal carrier DCO setting is 88540000/63 or 1450396·825Hz.

Formulation of Integrated Carrier Phase

Integrated carrier phase or integrated Doppler is used to smooth the code phase pseudo-ranges:

$$f_D = \frac{-v \times L_1}{c}$$

where f_D is the Doppler frequency and v the relative velocity. The integral of the Doppler frequency gives a measure of the range change over the integration interval:

$$\int f_D = -\int \frac{v \times L_1}{c}$$

$$f_D = f_{DCO} - f_{nom}$$

where f_{DCO} is the carrier DCO frequency (Doppler shifted) and f_{nom} is the nominal carrier DCO frequency (unshifted). Therefore:

$$\int f_{DCO} - \int f_{nom} = -\int \frac{v \times L_1}{c}$$

$$N_k - T \times f_{nom} = -\frac{L_1}{c \times \Delta R}$$

where N_k is the carrier DCO cycle count between TICs, T is the TIC interval and ΔR is the change in range between TICs. Hence,

$$\Delta R = \frac{c}{L_1 (T \times f_{nom} - N_k)}$$

A running sum of ΔR can then be used to smooth the code pseudo-ranges.

Determination of the Navigation Solution

The basic radial range measurement to satellite i is given by:

$$\sqrt{(x-x_i)^2+(y-y_i)^2+(z-z_i)^2} + ct = R_i$$

where (x,y,z) is the receiver location, (x_i,y_i,z_i) is the satellite position, t is the receiver clock offset and R_i the pseudo-range.

To solve for the 4 unknowns, (x,y,z) and t, 4 equations or pseudo-ranges to 4 satellites are required. Commonly, a linearised version of the range equation is used:

$$\Delta_{Ri} = \frac{(x-x_i)}{(R_{ni}-ct_n)}\Delta x + \frac{(y-y_i)}{(R_{ni}-ct_n)}\Delta x + \frac{(z-z_i)}{(R_{ni}-ct_n)}\Delta x + c\Delta t$$

where (x_n,y_n,z_n) and t_n are the nominal (best estimates) of (x,y,z) and t; Δx, Δy, Δz and Δt are the corrections to these estimates; R_{ni} is the nominal pseudo-range measurement and ΔR_i is the difference between the actual and nominal measurement.

The range equations can then be expressed in matrix notation by:

$$\boldsymbol{Ax} = \boldsymbol{r} \text{ or } \boldsymbol{x} = \boldsymbol{A}^{-1}\boldsymbol{r}$$

where $\boldsymbol{A}$ is the solution or design matrix (the direction cosine matrix), $\boldsymbol{x}$ is the receiver position and clock correction vector and $\boldsymbol{r}$ is the pseudo-range measurement difference vector.

More generally, for the overdetermined case (more than 4 satellites), the method of least squares is used:

$$\boldsymbol{Ax} - \boldsymbol{r} = \boldsymbol{v}$$

where v is the vector of residuals. Since the solution matrix is no longer square the generalised or pseudo-inverse must be used:

$$\boldsymbol{x} = (\boldsymbol{A}^T\boldsymbol{W}\boldsymbol{A})^{-1}\boldsymbol{A}^T\boldsymbol{W}\boldsymbol{r}$$

where $\boldsymbol{W}$ is the weight matrix.

It can be shown that the optimum value of $\boldsymbol{W}$ is the inverse covariance matrix of the pseudo- ranges. This can be estimated from the satellite URAs (User Range Accuracy) transmitted in the satellite data messages.

If the solution is underdetermined (only 3 measurements), or if the GDOP is above the desired GDOP mask, then altitude aiding is used by adding an extra measurement for an imaginary satellite at the centre of the Earth. The added pseudo-range is equal to the magnitude of the current receiver range vector from the Earth's centre.

Pseudo-range rates are used in the same manner as pseudo-ranges to determine the receiver velocity vector and clock drift.

GPS BUILDER-2 PERFORMANCE

OPERATION

GPS Builder-2 operates through a number of simple commands which can be entered via a command line or read from a file at start-up (or during normal operation). The system allows dynamic re-configuration of a number of the key receiver parameters, e.g. number of channels, operation masks, reference position, altitude aiding, use of integrated carrier, channel coasting, automatic or user selection of satellites etc.

Navigation and receiver status data can be saved to file in either a comma delimited text format or in RINEX2 format. GPS Builder-2 can accept and use RTCM SC-104 DGPS data through the PC COM port.

Dynamic Navigation.

Many function key selectable displays are provided, showing receiver and system data.

Screen Displays (Figs. 25-38)

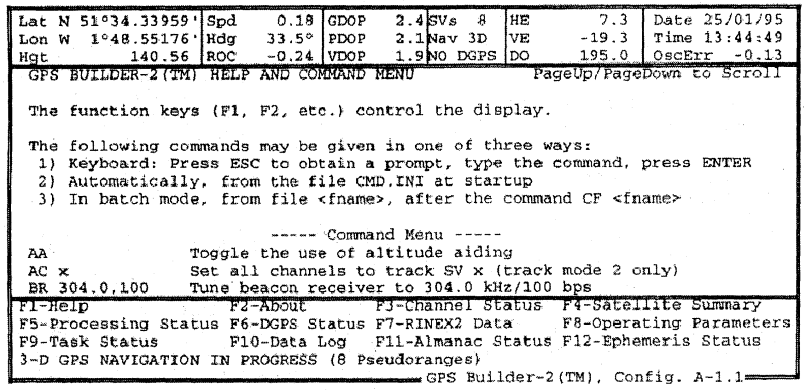


Fig. 25 Screen display 1: Help/Command menu (4 pages)

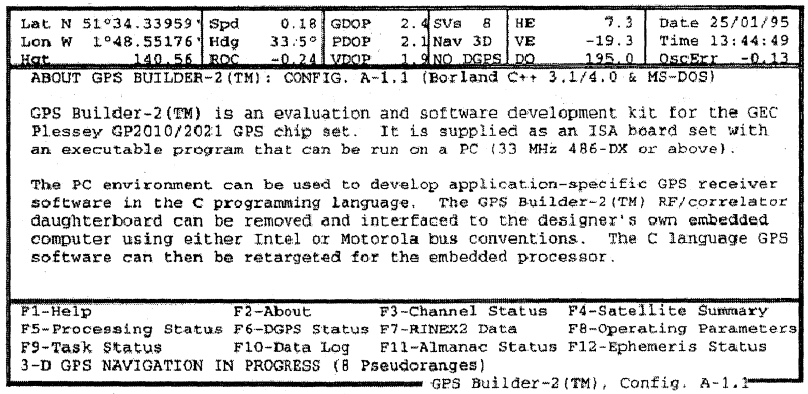


Fig. 26 Screen display 2: About GPS Builder-2

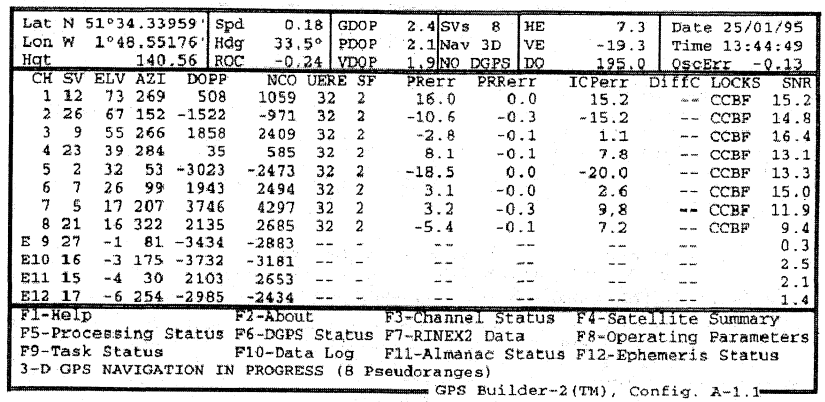


Fig. 27 Screen display 3: Channel status

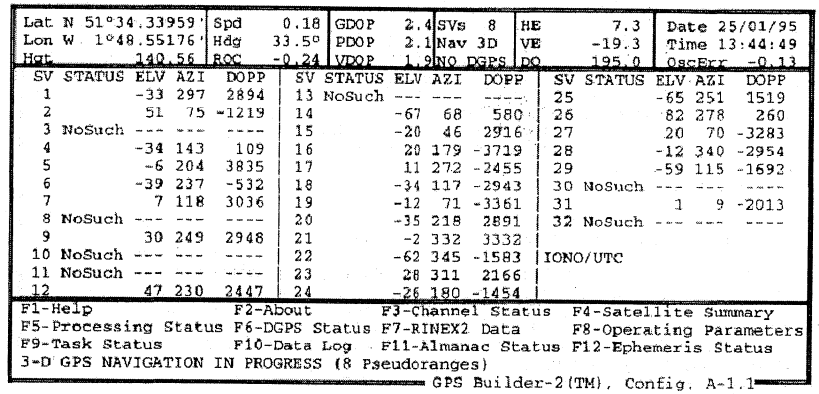


Fig. 28 Screen display 4: Satellite summary

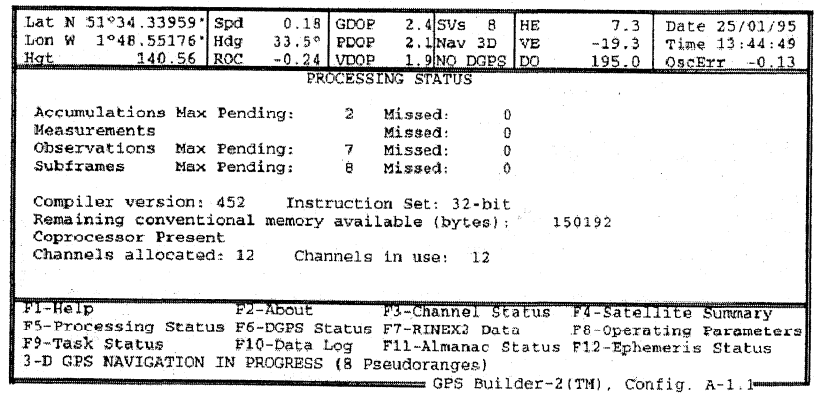


Fig. 29 Screen display 5: Processing status

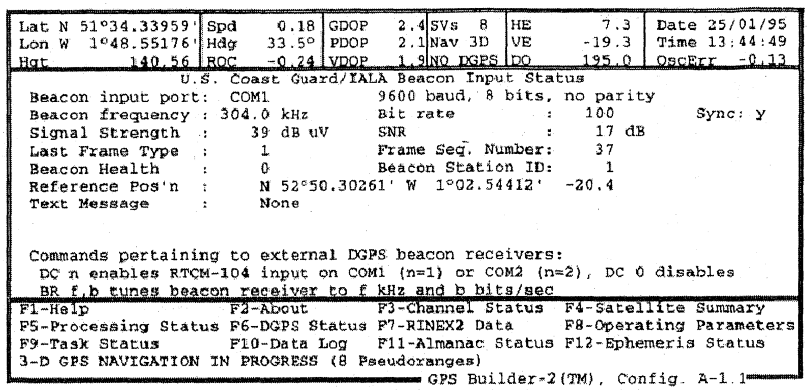


Fig. 30 Screen display 6: External beacon receiver status

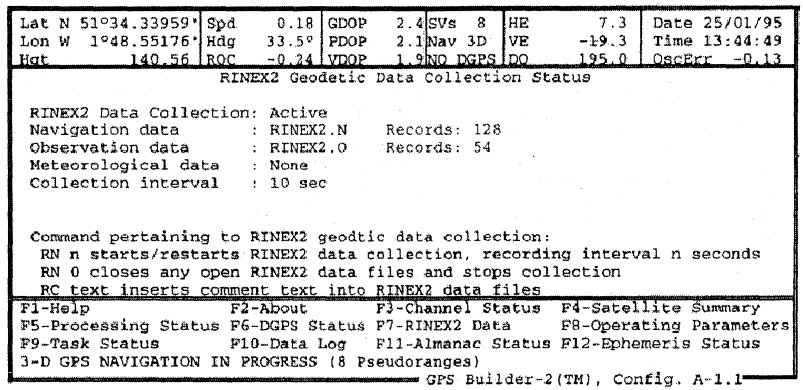


Fig. 31 Screen display 7: RINEX2 geodetic data collection status

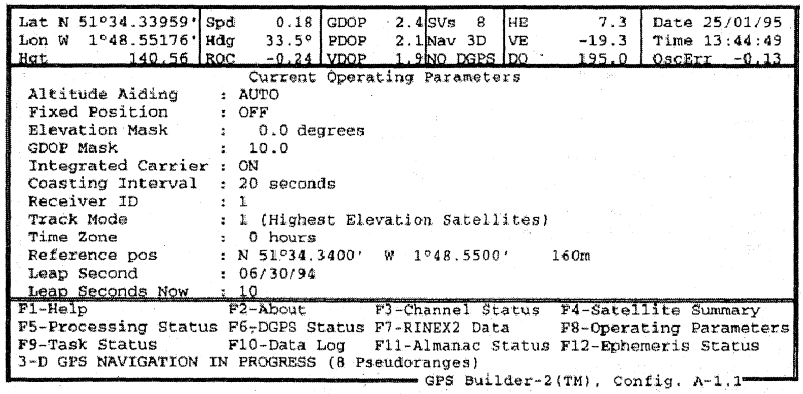


Fig. 32 Screen display 8: Operating parameters

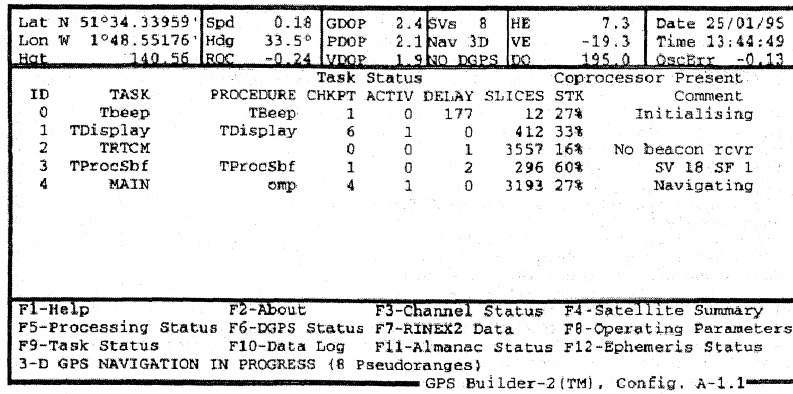


Fig. 33 Screen display 9: Task status

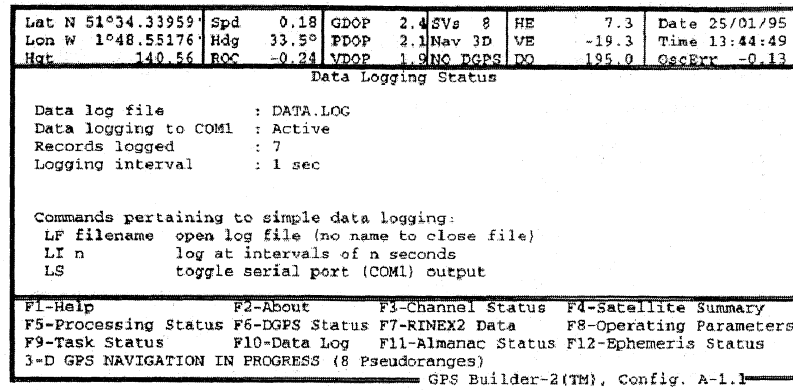


Fig. 34 Screen display 10: Data logging status

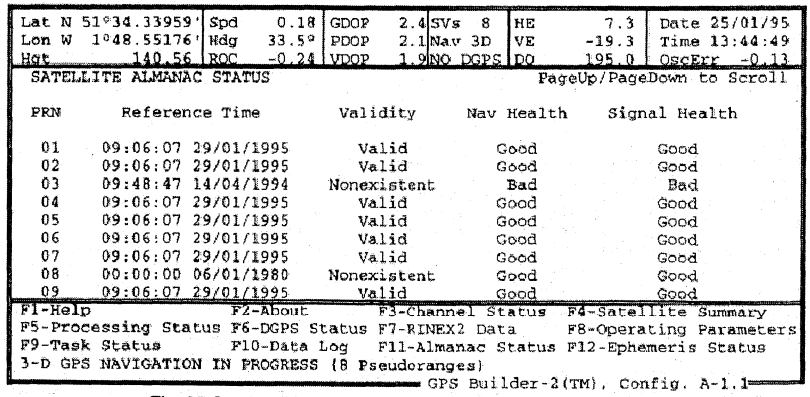


Fig. 35 Screen display 11: Satellite almanac status (summary)

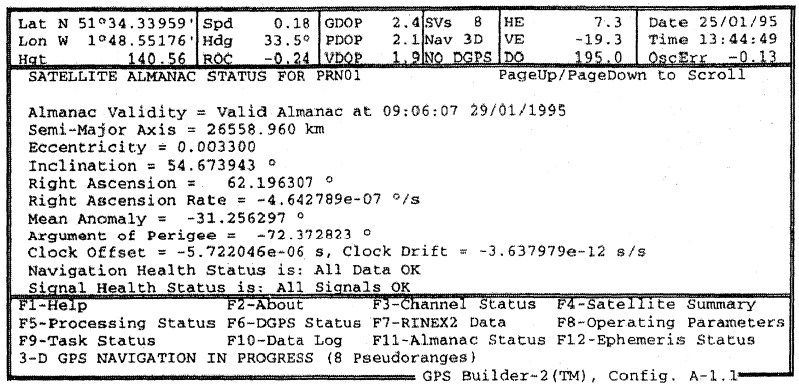


Fig. 36 Screen display 12: Satellite almanac status (detailed)

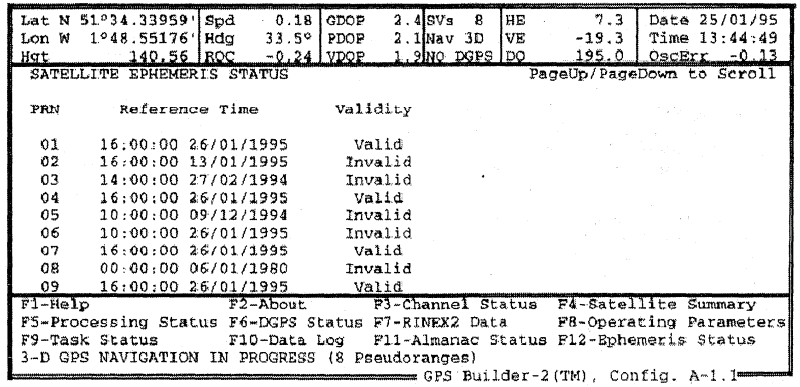


Fig. 37 Screen display 13: Satellite ephemeris status (summary)

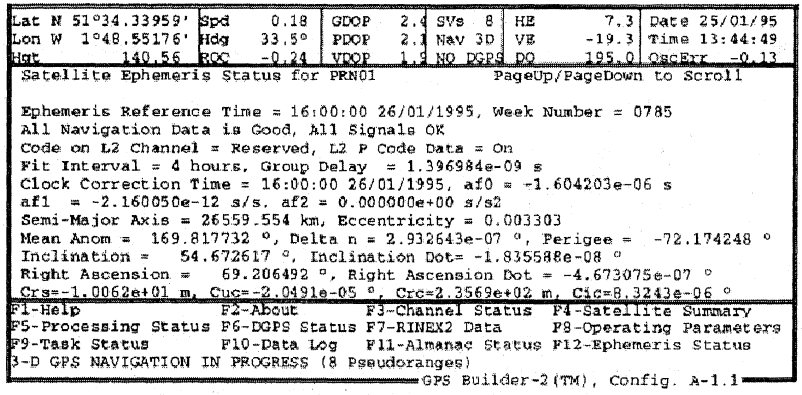


Fig. 38 Screen display 14: Satellite ephemeris status (detailed)

Performance Parameters

SV selection strategy

The SV selection strategy (i.e. which satellites the receiver tries to acquire) can be complex, and not always successful. If the number of receiver channels is less than the number of visible satellites (or satellites above the receiver elevation mask) then decisions have to be made about which satellites to acquire.

A common criterion for selection is those satellites which give the smallest dilution of precision in the navigation fix. This is fine if the receiver antenna has full sky visibility but if there are obstructions shielding the satellites from the antenna (particularly relevant in dynamic applications) then either some complex software is required to swap satellites in and out of the acquisition loop or worse still, the receiver may stick to the 'optimum' constellation until either the satellites eventually become visible or the best constellation changes. The number of satellites above the horizon is obviously a position and time dependent quantity.

However, for reasonable latitudes (say below ±60°), the average number of visible satellites will be about 8 and on occasions will increase to 10, 11 or even 12. Hence, having enough receiver channels as visible satellites means that all satellites can be tracked (or at least acquisition can be attempted) without the need for a complex or time consuming selection strategy.

In GPS Builder-2, when sufficient data is available, the initial satellite-to-channel allocation is based in descending elevation angle and then this is updated as satellites rise and set. The ability to track all visible satellites ('all-in-view') also adds to the position accuracy and availability.

Signal Acquisition Times

The initial signal acquistion time for a particular satellite in GPS Builder-2 is determined by how many frequency bins have to be searched to find the signal. The number of bins is determined by the bin width and the maximum frequency excursions due to the satellite receiver relative motion and the receiver clock error. For a static receiver the maximum Doppler excursion is about ±5kHz.

The reference oscillator used with GPS Builder-2 is a Rakon™ TXO4010 with the following stability:

Temperature :	±2·5 ppm (−30 to +75°C)
Supply voltage :	±0·2 ppm (+5V±5%)
Ageing :	±1·0 ppm/year

Assuming a total reference oscillator error of ±4 ppm i.e. ±6·3kHz at $L1$ plus the Doppler error of ±5·0kHz gives a total frequency excursion of about ±11·3kHz.

For the GPS Builder-2 frequency bin width of 500Hz a total of 45 bins exists. For a 4-second bin search time this gives a total of 180 seconds to cover the complete range. However, if the clock error is known (but no estimate of receiver or satellite positions) then this decreases the search window to ±5·0kHz, the number of bins to 20 and the search time to 80 seconds (worst case).

If the satellite almanacs, the reference clock error and a reasonable estimate of the receiver position and current time (errors of 1·3Hz per km of position error and 0·9Hz per second of time error) are available then it should be possible to constrain the search within 1 to 3 bins, giving an acquisition time of 4 to 12 seconds.

Bit And Frame Sync Times

Following signal acquisition, the next step is bit and frame sync. A minimum of 2 seconds dwell time is required for bit sync to the data transitions. To achieve frame sync the TLM and HOW words need to be successfully received and the 20ms Epoch Counter set.

If valid data is being logged (continuous reception and no parity errors), then TLM and HOW reception will take between 1·2 and 7·2 seconds. If the 20ms Epoch Counter is slewed then frame sync will be delayed 6 seconds.

Hence, to go from code/carrier lock to bit and frame sync will normally take between about 3 and 15 seconds.

Signal Re-Acquisition Times

When a signal is lost, the tracking loops for the channel concerned go into a coast mode. In this mode the code and carrier DCOs are left free running at their current values for the duration of the maximum coasting interval (user configurable) or until the code and carrier detection thresholds are exceeded. If the maximum coasting interval is exceeded, the channel returns to the search mode. If the signal reappears (e.g., after being temporarily obstructed by a building) within the maximum coasting interval then signal reacquisition typically occurs within 1 second.

Time-To-First-Fix

TTFF is dominated by how much initial information GPS Builder-2 has. Note: The satellite almanacs and ephemerides can be read from file and the clock frequency error and initial position estimate supplied via command line.

If no information is available (i.e., position estimate, time estimate, reference oscillator error, satellite almanacs and ephemerides) then a sky search occurs, selecting satellites sequentially from their PRN ordering. In this scenario, TTFF is typically 3 to 6 minutes*.

If GPS Builder-2 has satellite almanacs, a reasonable time and position estimate and a reference oscillator error estimate (the usual scenario) then TTFF is typically less than 1 minute.* Note that it can take 30 seconds to receive an ephemeris.

If GPS Builder-2 has the above information and valid (less than 4 hours old) satellite ephemerides then TTFF is typically less than 30 seconds*.

*These figures assume a static receiver and unobstructed sky visibility.

STATIC NAVIGATION

Fig. 39 shows a GPS Builder-2 position fix scatter plot where 10 satellites are included in the solution. Fig. 40 shows position fixes over the same period but for a non-GPS Builder 2 system using only the 'best' four satellites. A comparison of these plots clearly demonstrates the benefit to position fix accuracy of 'all-in-view' used by GPS Builder-2.

Fig. 41 shows what sort of position fix accuracy can be achieved when S/A is inactive (no DGPS corrections applied). Fig. 42 shows the number of satellites tracked during this period.

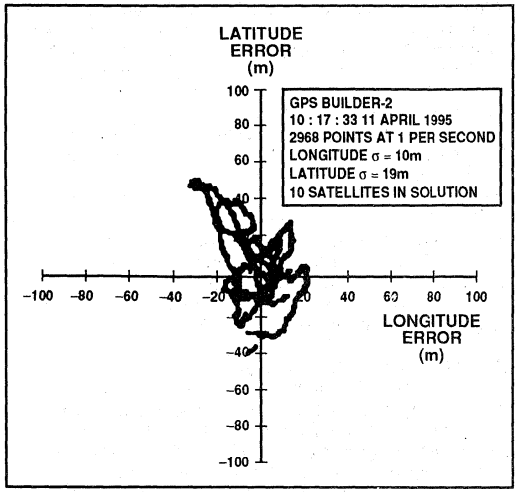


Fig. 39 Static navigation using GPS Builder-2, S/A active

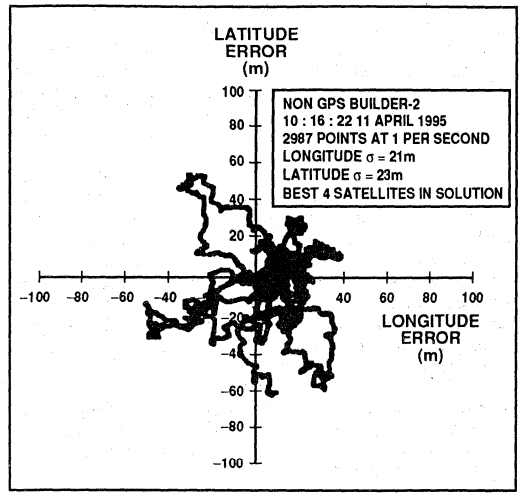


Fig. 40 Static navigation using competitive product, S/A active

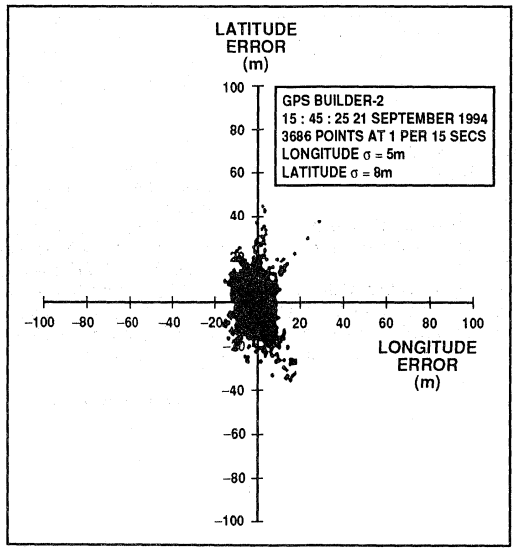


Fig. 41 Static navigation, S/A inactive

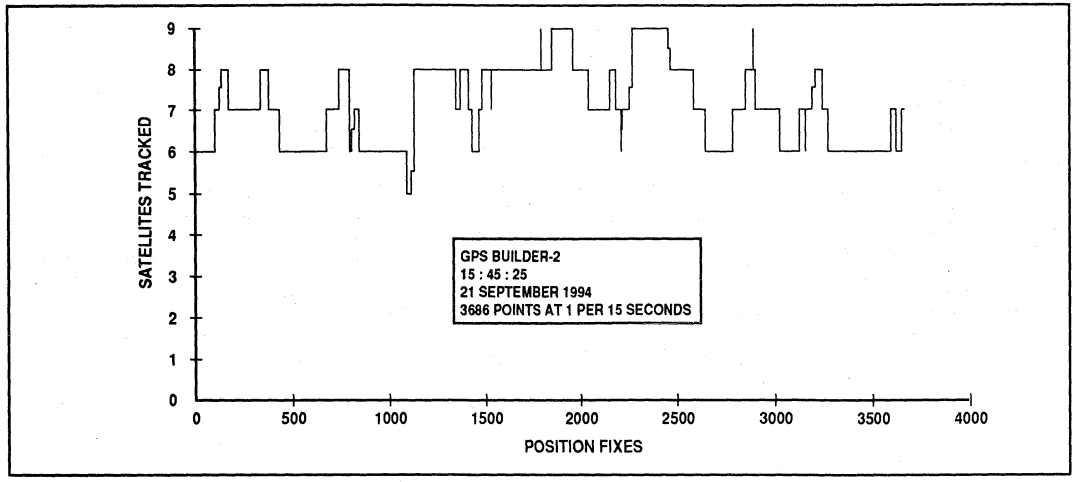


Fig. 42 Number of satellites tracked

GPS BUILDER-2 ENHANCEMENTS

GPS Builder-2 is a generalised solution to the GPS receiver problem. To maintain a high level of clarity, generality and adaptability, no real attempts have been made to target the solution for one particular application area. This provides numerous opportunities for customisation to user-specific applications.

Such areas include:

(i) Acquisition times. Acquisition/re-acquisition times can be improved by using both the Prompt and Track arms of the correlator in the acquisition search. This could involve stepping the code phase as opposed to a sliding search. Also, bit and frame sync times can be shortened by using all the available information to determine epoch settings.

(ii) Navigation filter. GPS Builder-2 does not use a navigation filter, as this is a very application-specific function to get optimum results.

(iii) Additional aiding. In applications where GPS is not sufficient as the sole means of navigation information then the navigation solution could contain aiding from external sources (e.g. gyroscopic sensor).

GLOSSARY

AGC	Automatic Gain Control
Almanac	A low precision ephemeris
ASCII	American Standard Code for Information Interchange
Bin	Carrier frequency step during signal acquisition
C/A Code	Coarse/Acquisition code
Chip	One bit of satellite code (C/A code has 1023 chips)
CW	Continuous Wave
DCO	Digitally Controlled Oscillator
DGPS	Differential Global Positioning System
EML	Early Minus Late
Ephemeris	Orbital parameter set for high precision satellite position prediction
Epoch	Code repetition interval (C/A code epoch is 1ms)
EPROM	Erasable Programmable Read-Only Memory
E^2PROM	Electrically Erasable Programmable Read-Only Memory
FIFO	First-In, First-Out register
FLL	Frequency Locked Loop
GDOP	Geometric Dilution Of Precision
GLONASS	Global Orbiting Navigation Satellite System
GPS	Global Positioning System
HDOP	Horizontal Dilution Of Precision
HOW	Hand-Over Word
IF	Intermediate Frequency
ISA	Industry Standard Architecture
LNA	Low Noise Amplifier
NMEA	National Marine Electronics Association
NVM	Non-Volatile Memory
PDOP	Position Dilution Of Precision
PLD	Programmable Logic Device
PLL	Phase Locked Loop
PRN	Pseudo-Random Noise
PROM	Programmable Read-Only Memory
RAM	Random Access Memory
RISC	Reduced Instruction Set Computer
RINEX	Receiver-Independent Exchange format
ROM	Read-Only Memory
RTC	Real Time Clock
S/A	Selective Availability
SAW filter	Surface Acoustic Wave filter
SV	Space Vehicle, i.e. satellite
TCXO	Temperature Compensated Crystal Oscillator
TIC	A signal of programmable period which is used to sample and latch tracking module measurement data
TLM	Telemetry
TTFF	Time To First Fix
UART	Universal Asynchronous Receiver/Transmitter
URA	User Range Accuracy
UTC	Universal Time Co-ordinated
VCO	Voltage Controlled Oscillator
VDOP	Vertical Dilution Of Precision

Section 2
RF Products

GP2010

GLOBAL POSITIONING SYSTEM RECEIVER RF FRONT END

The GP2010 is GEC Plessey Semiconductors' second generation RF Front-end for Global Positioning System (GPS) receivers. The GP2010 uses many innovative design techniques and a leading-edge bipolar process to offer a lower power, lower cost and higher reliability RF solution than existing discrete or gallium-arsenide designs. The GP2010 is designed to operate from either 3 or 5 Volt power supplies.

The input to the device is the L1 (1575.42MHz) Coarse-Acquisition (C/A) code Global Positioning signal from an antenna (via a low-noise pre-amplifier). The output is 2-bit quantised for subsequent signal processing in the digital domain. The GP2010 contains an on-chip synthesiser, mixers, AGC and a quantiser which provides Sign and Magnitude digital outputs. A minimum of external components is required to make a complete GPS front-end.

The device has been designed to operate with the GP2021 12-channel Global Positioning Correlator, and DW9255 SAW filter, both also available from GEC Plessey Semiconductors.

FEATURES

- Low Voltage Operation (3V - 5V)
- Low Power - 200mW typ. (3V supply)
- C/A Code Compatible
- On-chip PLL Including Complete VCO
- Triple Conversion Receiver
- 44-Lead Surface Mount Quad Flat-Pack Package
- Sign and Magnitude Digital Outputs
- Compatible with GP2021 CMOS Correlator

APPLICATIONS

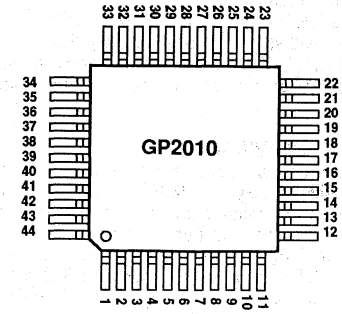
- C/A Code Global Positioning by Satellite Receivers
- Time Standards
- Navigation
- Surveying

ORDERING INFORMATION

The GP2010 is available in 44 pin Quad Flat pack (gullwing formed leads) in both Commercial (0°C to +70°C) and Industrial (-40°C to +85°C) grades. The ordering codes below are for standard screened devices.

ORDERING CODE

GP2010 CG GPBR Commercial - Plastic 44-pin PQFP
GP2010 IG GPBR Industrial - Plastic 44-pin PQFP



Pin	Name	Pin	Name
1	IF Output	23	V_{CC} (DIG)
2	PLL Filter 1	24	REF 2
3	PLL Filter 2	25	REF 1
4	V_{EE} (OSC)	26	V_{CC} (RF)
5	V_{CC} (OSC)	27	V_{EE} (RF)
6	V_{EE} (OSC)	28	V_{EE} (RF)
7	V_{EE} (REG)	29	RF Input
8	PREF	30	V_{EE} (RF)
9	PRESET	31	V_{EE} (RF)
10	V_{EE} (IO)	32	V_{CC} (RF)
11	CLK	33	O/P 1-
12	MAG	34	O/P 1+
13	SIGN	35	V_{CC} (2)
14	OPC_{IK-}	36	I/P 2-
15	OPC_{IK+}	37	I/P 2+
16	V_{DD} (IO)	38	V_{EE} (IF)
17	PD_N	39	V_{EE} (IF)
18	TEST	40	O/P 2-
19	LD	41	O/P 2+
20	V_{EE} (DIG)	42	V_{CC} (3)
21	AGC -	43	I/P 3-
22	AGC +	44	I/P 3+

Fig. 1 Pin connections - top view

RELATED PRODUCTS AND PUBLICATIONS

Part	Description	Data Reference
DW9255	35.42MHz SAW Filter	DS3861
GP2021	Twelve-Channel Correlator	DS4057
GPSBuilder	Twelve-Channel GPS receiver development system	DS4004

ABSOLUTE MAXIMUM RATINGS (Non-simultaneous)

Max. Supply Voltage	7V
Max. RF Input	+15dBm
Max. voltage on any pin	V_{CC}/V_{DD} + 0.5V
except LD (pin 19) and PReset (pin 9), which are 5.5V	
Min. voltage on any pin	V_{EE} - 0.5V
Storage Temperature	-65°C to +150°C
Operation Junction Temperature	-40°C to +150°C
10MHz Reference Input	1.5V pk -pk

ESD PROTECTION

The GP2010 device is static sensitive, the most sensitive pins withstand a 750V test by the human body model. Therefore, ESD handling precautions are essential to avoid degradation of performance or permanent damage to this device.

PRODUCT DESCRIPTION

The GP2010 is a complete front-end down-converter for Global Positioning System (GPS) receivers. It is a state-of-the-art design combining an on-chip PLL synthesiser at 1400MHz, a low-noise amplifier, 3 mixers, and a 2-bit A to D converter. The GP2010 receives the 1575.42MHz signal transmitted by GPS satellites and converts it to a 4.309MHz IF, using a triple down-conversion. The 4.309MHz IF is sampled to produce a 2-bit digital output. If the GP2010 is used in conjunction with the GP2021 correlator, then the GP2021 provides a sampling clock of 5.714MHz. This converts the IF to a 1.405MHz 2-bit digital output at TTL levels.

The GP2010 can operate from a single supply from +3V (nominal) to +5V (nominal).

A block diagram of the circuit is shown in figure 2.

IF STRIP

The input signal to the GP2010 is the GPS L1 signal received via an antenna and a suitable LNA. The L1 input is a spread spectrum signal at 1575.42MHz with 1.023Mbps BPSK modulation. The signal level at the antenna is about -130dBm, spread over a 2.046MHz bandwidth, so the wanted signal is actually buried in noise. The high RF input compression point of the GP2010 means that with subsequent IF filtering it is possible to reject large out of band jamming signals, in particular 900MHz as used by mobile telephones. The on-chip PLL generates the first local-oscillator frequency at 1400MHz. The output of the front-end mixer (Stage 1) at 175.42 MHz can then be filtered before being applied to the second stage. The double-balanced stage 1 mixer outputs are open-collectors, and require external dc bias to V_{CC}.

The second stage contains further gain and a mixer with a local oscillator signal at 140 MHz giving a second IF at 35.42 MHz. The second stage mixer is also double-balanced with open-collector outputs requiring external dc bias to V_{CC}.

The signal from stage 2 is passed through an external filter with a 1dB bandwidth of 1.9MHz. The performance of this filter is critical to system performance and it is recommended that a SAW filter is used (part number DW9255, also available from GEC Plessey Semiconductors). The output of the filter then feeds the main IF amplifier. This includes 2 AGC amplifiers and a third mixer with a local oscillator signal at 31.111 MHz giving a final IF at 4.309 MHz. There is an on-chip filter after the third mixer which provides filtering centred on 4.309 MHz. The IF output, which has 1kΩ output impedance, is provided for test purposes. All of the signals within the IF amplifier are differential including the filter inputs and outputs, except the IF output (pin 1), to reduce any common mode interference.

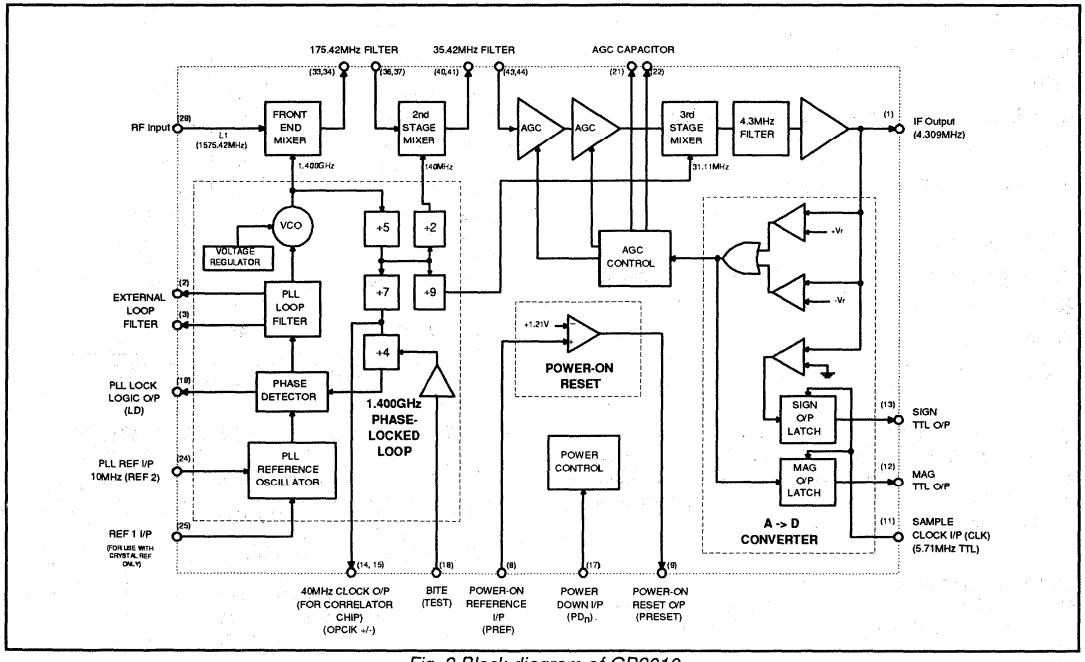


Fig. 2 Block diagram of GP2010

The IF output is fed to a 2-bit quantiser which provides sign and magnitude (MSB and LSB) outputs. The magnitude data controls the AGC loop, such that on average the magnitude bit is set (high) 30% of the time. The AGC time constant is set by an external capacitor.

The sign and magnitude data, SIGN (pin 13) and MAG (pin 12), are latched by the rising edge of the sample clock, CLK (pin 11), which is normally derived from the correlator; the GP2021 provides a 5.714MHz (=40/7) clock, giving a sampled IF centred on 1.405MHz.

The Digital Interface circuits use a separate power-supply, V_{DD}(IO), which would normally be shared with the correlator to minimise crosstalk between the analog and digital sections of the device.

ON-CHIP PHASE-LOCKED LOOP SYNTHESISER

All of the local oscillator signals are derived from an on chip phase locked loop synthesiser. This includes a 1400MHz VCO complete with on-chip tank circuit, dividers and phase detector, with external loop filter components. A 10.000MHz reference frequency is required for the PLL. This can be achieved by attaching an external 10.000MHz crystal to the on-chip PLL reference oscillator (see figure 5). However in most applications the user will need an external source, such as a TCXO, to provide greater frequency stability (see figure 6). An external reference should be ac coupled to REF2 (pin 24); REF 1 (pin 25) should be left open circuit.

The three local oscillator signals 1400MHz, 140.0MHz and 31.11MHz are derived from the 1400MHz synthesiser output. The synthesiser also provides a 40 MHz balanced differential output clock (pins 14 & 15) which can be used to clock the GP2021 correlator. The clock is a low level differential signal which helps minimise interference with the analog areas of the circuit. A PLL lock-detect output, LD (pin 19), is also provided, which is logic high when the PLL is phase-locked to the 10.000MHz reference signal.

The VCO power-supply incorporates an on-chip regulator to improve the noise-immunity of the PLL. This feature is only available when operating with a 5 volt (nominal) supply which is regulated to 3.3 volts internally. This internal regulated supply is referenced to V_{CC}(OSC) (pin 5). Figure 7 shows the required connections for both 3 volt and 5 volt operation.

A further feature of the circuit is the TEST input (pin 18). When this input is held high the PLL is unlocked with the VCO at its maximum frequency.

POWER-DOWN CAPABILITY

A power down function is provided on the GP2010, to limit power consumption. This powers down the majority of the circuit except the "power-on reset" function (see below).

If the power down feature is not required, the Power-down input, PD_n (pin 17), should be connected to 0V dc (=Vee/Ground).

POWER-ON RESET FUNCTION

The GP2010 includes a voltage detector which operates from the digital interface supply. This circuit is used to produce a TTL logic low output while the GPS receiver power supply is switching on, and produces a logic high output when the power supply voltage has achieved a nominal value. This output can be used to disable the GP2021 correlator while the power supply is switching on. An internal bandgap reference of approximately +1.21V is compared with the voltage on a sense pin, PREF (pin 8); when the voltage on this pin exceeds the reference, a TTL logic high level appears at the Power-on Reset output, PRESET (pin 9). Thus, if the sense input voltage is derived from an external resistive divider from the Digital Interface supply, V_{DD}(IO) (pin 16), such that the sense voltage at nominal V_{CC} is V_S, then the supply threshold, Vcc(thresh), at which the PRESET output goes to logic high is:-

$$V_S = \frac{V_{CC}\ (\text{nom}) \times 1.21}{V_{CC}\ (\text{thresh})}$$

For a V_{CC} (nom) of 5.0V, V_{CC} (thresh) may be set to approx. 4.0V, giving V_S of 1.5V.

For a V_{CC} (nom) of 3.0V, V_{CC} (thresh) may be set to approx. 2.4V, giving V_S of 1.5V.

ADDITIONAL INFORMATION

All the digital inputs and outputs can use a separate power supply to help prevent digital switching transitions interacting with the analog sections of the device, and as an additional precaution, the digital inputs and outputs are on the opposite side of the device to the critical analog pins.

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions (see Fig. 3 for test circuit):

Industrial (I) grade: T_{AMB} = -40°C to +85°C
Supply voltage: V_{CC} and V_{DD} = +2.7V to +5.5V (both grades)

Test conditions (unless otherwise stated):

Supply voltages: V_{CC} = +2.7V and +5.5V, V_{DD} = +2.7V and +5.5V
Test temperature: Industrial (I) grade product: +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
SUPPLY CURRENT					
Normal mode - Analog interface		55	77	mA	Pins 5, 23, 26, 32, 35, 42
- Digital interface		9	14.5	mA	Pin 16
Power down mode - Analog interface		3	6	mA	Pins 5, 23, 26, 32, 35, 42
- Digital interface		3	5	mA	Pin 16
Power Supply Differential			100	mV	Between any V_{CC}/V_{DD} pins (Note 7)
Power down Response time		3		µs	(Note 7)
IF STRIP					
Front End/Mixer 1					
Conversion Gain (G1)	11	18	25	dB	R_O = 600Ω (Note 2)
					F_{IN} = 1575.42MHz
Noise Figure		9		dB	Z_S = 50Ω (Note 7)
Input Compression (1dB)	-22	-16		dBm	
Input Impedance		15		Ω	Pin 29 (Notes 1 and 7)
		3.6		nH	(Notes 1 and 7)
Differential Output Impedance		700		Ω	Pins 33 & 34 (Note 8)
RF Input Image Rejection		8		dB	F_{IN} = 1224.58MHz (Note 7)
Stage 2/Mixer 2					
Conversion Gain (G2)	22	27	33	dB	F_{IN} = 175.42MHz
Input Compression (1dB)	5	14		mV rms	
Differential Input Impedance		700		Ω	Pins 36 & 37 (Note 8)
Differential Output Impedance		500		Ω	Pins 40 & 41 (Note 8)
Stage 3					
High Gain (In terms of total strip)	106-G1-G2			dB	(Note 6)
High Gain (G3)		75		dB	F_{IN} = 35.42MHz
Gain Control Range		60		dB	(Note 3)
Differential Input Impedance		1		kΩ	Pins 43 & 44 (Note 8)
IF Output amplitude	60	85	120	mV rms	CW input (Note 3)
IF Output impedance		1		kΩ	Pin 1(Note 8)
4.3MHz Filter Response					
Flatness 4.3 ± 1MHz	-1.5		+1.0	dB	
Rejection @ 0.5MHz		14		dB	(Note 7 and 9)
@ 50MHz	45	70		dB	
2 BIT QUANTISER					
Sign Duty Cycle	40	50	60	%	} (Note 10)
Mag Duty Cycle	20	30	40	%	
AGC Time Constant		2		ms	C_{AGC} = 100nF
ON_CHIP PLL SYNTHESISER					
Phase Noise					15kHz Loop Bandwidth
± 1kHz		-68		dBc/Hz	} (Note 7)
± 10kHz		-75		dBc/Hz	
± 100kHz		-88		dBc/Hz	
± 1MHz		-110		dBc/Hz	
± 5MHZ		-120		dBc/Hz	
± 50MHz		-120		dBc/Hz	
PLL Spurs		-50		dBc	(Note 7)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
VCO Maximum Lock Frequency	1414			MHz	
VCO Minimum Lock Frequency			1386	MHz	
VCO regulator output voltage	3	3.3	3.5	V	(Note 4)
VCO Gain	50	150	240	MHz/V	
Phase Detector Gain		5.3		V/rad	(Note 7)
10MHz Reference Input	0.1	0.6	1.2	V pk-pk	Pin 24
10MHz Reference Input Impedance		5		kΩ	(Note 11)
PLL Lockup Time		6		ms	From Power up (Note 7)
PLL Loop Gain		150		dB	(Note 7)
DIGITAL INTERFACES					
Sample Clock, Power Down, Test Inputs.					Pins 11, 17, 18
V_{IH}	2		V_{DD}	V	
V_{IL}	0		0.5	V	
Input Current High I_{IH}			10	µA	$V_{IH} = V_{DD}$
Input Current Low I_{IL}	-300			µA	$V_{IL} = V_{EE}$
Sign/Mag Outputs					Pins 13, 12
V_{OH}	V_{DD}-1			V	I_O = -0.5mA
V_{OL}			0.5	V	I_O = 0.5mA
Sample Clock to Sign/Mag Delay		20		ns	CL = 15pF, RL = 15kΩ (Note 7)
40MHz Clock Output					
High Level (V_{OH})	V_{DD}-1.25	V_{DD}-1	V_{DD}-0.8	V	Pins 14 & 15
Low Level (V_{OL})		V_{OH}-0.1		V	(Note 5)
Output (differential)	150	220		mV p-p	CL = 15pF (GND) (Note 7)
					CL = 5pF (Diff) (Note 7)
Duty Cycle		43		%	(Note 7)
LD (PLL Lock)/PRESET Outputs					Pins 19 and 9
Low Level (V_{OL})		0.2	0.5	V	I_O = 0.5mA
High Level (V_{OH})	V_{DD}-1	V_{DD}		V	I_O = -10µA
Power-on reset comparator input					Pin 8
Power Reset Threshold Level	1.1	1.21	1.35	V	
Power Reset Reference Input Current	-10		10	µA	

Notes On Electrical Characteristics:- All RF measurements are made with appropriate matching to the input or output impedances, such as balun transformers, and levels refer to matched 50ohm ports (see figure 3 for test circuit)

1. RF input impedance (series) without input matching components connected.
2. Input matched to 50ohm, output loaded wlth 600ohms differential
3. Maximum Stage 3 input signal amplitude for correct AGC operation = 20mV rms.
4. VCO regulator voltage measured with respect to Vcc (OSC) - pin 5.
5. OPCLK outputs are differential and are referenced to V_{DD}.
6. Minimum gain requirement expressions:

$$-7dBm < -174dBm/Hz + 19dB + G1 + G2 + G3 - 21dB + 63dB$$

where -7dBm = typical IF Output level with AGC active (equivalent to 100mV rms)
-174dBm/Hz = background noise level at RF input
19dB = sum of LNA gain and noise figure
-21dB = total loss in 175MHz and 35MHz filters
63dB = summation of noise over a 2MHz bandwidth

Rearranging the above expression gives G1 + G2 + G3 > 106dB.

7. This parameter is not production tested.
8. This impedance is toleranced at +/-30% and is not production tested.
9. Roll off occurs in on-chip capacitive coupling IF Output to input of ADC circuit. Not measurable at IF Output.
10. CW input on pins 43 & 44 of 35.42MHz at 7mV rms.
11. This input impedance applies to the typical input level. The impedance is level dependent and is not tested or guaranteed.

PIN DESCRIPTIONS

All V_{EE} and V_{CC}/V_{DD} pins should be connected to ensure reliable operation

Pin No.	Signal Name	Input/Output	Description
1	IFOutput	Output	IF Test output. Connected to output of Stage 3 prior to the A to D converter. A series 1kΩ resistor is incorporated for buffering purposes.
2	PLL Filt1	Output	PLL Filter 1. Connected to the bias network within the on-chip VCO. An external PLL loop filter network should be connected between this pin and PLL Filt 2 (see below).
3	PLL Filt2	Output	PLL Filter 2. Connected to the varactor diodes within the on-chip VCO. An external PLL loop filter network should be connected between this pin and PLL Filt 1 (see above).
4,6	V_{EE} (OSC)	Input	Negative supply to the on-chip VCO. (See Note 1)
5	V_{CC} (OSC)	Input	Positive supply to the on-chip VCO.
7	V_{EE} (REG)	Input	Negative supply to the VCO regulator. This must be connected to GND.
8	PREF	Input	Power-on Reset Reference input. An on-chip comparator produces a logic HI when the PRef input voltage exceeds +1.21V.
9	PRESET	Output	Power-on Reset Output. A TTL compatible output controlled by the Power-on reset comparator (See above). This output remains active even when the chip is powered down. (See pin 17 - PDn).
10	V_{EE} (IO)	Input	Negative supply to the Digital Interface. (See Note 2)
11	CLK	Input	Sample Clock input from the correlator chip. A TTL compatible input (which operates at 5.714MHz if used with GP2021 correlator device) used to clock the MAG & SIGN output latches, on the **rising** edge of the CLK signal.
12	MAG	Output	Magnitude bit data output. A TTL compatible signal, representing the *magnitude* of the mixed down IF signal. Derived from the on-chip 2-bit A to D converter, synchronised to the CLK input clock signal.
13	SIGN	Output	Sign bit data output. A TTL compatible signal, representing the *polarity* of the mixed down IF signal. Derived from the on-chip 2-bit A to D converter, synchronised to the CLK input clock signal.
14	OPClk-	Output	40MHz Clock output - inverse phase. One side of a balanced differential output clock, with opposite polarity to Pin 15 - OPClk+. Used to drive a master-clock signal within the correlator chip.
15	OPClk+	Output	40MHz Clock output - true phase. Other side of a balanced differential output clock set, with opposite polarity to Pin 14 - OPClk-. Used to drive a master-clock signal within the correlator chip.
16	V_{DD} (IO)	Input	Positive supply to the Digital Interface. (See Note 2)

Pin No.	Signal Name	Input/Output	Description
17	PDn	Input	Power-Down control input. A TTL compatible input, which when set to logic high, will disable ALL of the GP2010 functions, except the power-on reset block. Useful to reduce the total power consumption of the GP2010. If this feature is not required, the pin should be connected to 0V (V_{EE}/GND).
18	TEST	Input	Test control input - Disable PLL. A TTL compatible input, which when set to logic high, will disable the on-chip PLL, by disconnecting the divided-down VCO signal to the phase-detector. The VCO will free run at its upper range of frequency operation. If this feature is not required, the pin should be connected to 0V (V_{EE}/GND).
19	LD	Output	PLL Lock Detect output. A TTL compatible output, which indicates if the PLL is phase-locked to the PLL reference oscillator. Will become logic high only when phase-lock is achieved.
20	V_{EE} (DIG)	Input	Negative supply to the PLL and A to D converter.
21	AGC-	Output	AGC Capacitor output - inverse phase. One side of a balanced output from the AGC block within IF Stage 3, to which an external capacitor is connected to set the AGC time-constant.
22	AGC+	Output	AGC Capacitor output - true phase. One side of a balanced output from the AGC block within IF Stage 3, to which an external capacitor is connected to set the AGC time-constant.
23	V_{CC} (DIG)	Input	Positive supply to the PLL and A to D converter.
24	REF 2	Input	10.000MHz PLL Reference signal input . Input to which an externally generated 10.000MHz PLL reference signal should be ac coupled, if an external PLL reference frequency source (e.g TCXO) is used (see fig. 6). If no external reference is used, this pin forms part of the on-chip PLL reference oscillator, in conjunction with an external 10.000MHz crystal (see fig. 5).
25	REF 1	Input	PLL reference oscillator auxillary connection. Used in conjunction with Pin 24 (REF 2) to allow a 10.000MHz external crystal to provide the PLL reference signal if no external PLL reference frequency source (e.g TCXO) is used. This pin should NOT be connected if an external TCXO is being used (see fig. 5).
26, 32	V_{CC} (RF)	Input	Positive supply to the RF input and Stage 1 IF mixer. Both pins 26 & 32 (V_{CC} (RF)) are connected internally, but must both be connected to V_{CC} externally, to keep series inductance to a minimum.
27, 28, 30, 31	V_{EE} (RF)	Input	Negative supply to the RF input and Stage 1 IF mixer. Pins 27, 28, 30 & 31 are all connected internally, but must ALL be connected to 0V (V_{EE}/GND) externally, to keep series inductance to a minimum.

Pin No.	Signal Name	Input/Output	Description
29	RF Input	Input	RF input. The GPS RF input signal @ 1575.42MHz from an external antenna with LNA and filter is connected to this pin via an input-matching network (see fig.4).
33	O/P 1-	Output	Stage 1 mixer output @ 175.42MHz - inverse phase. One of a balanced output from first stage IF mixer, to which one input of an external balanced 175MHz bandpass filter is connected. External dc biasing is required via an inductor connected to V_{CC}(RF) - the value of which is dependent on the filter used.
34	O/P 1+	Output	Stage 1 mixer output @ 175.42MHz - true phase. Second of a balanced output from first stage IF mixer, to which the second input of an external balanced 175MHz bandpass filter is connected. External dc biasing is required via an inductor connected to V_{CC}(RF) - the value of which is dependent on the filter used.
35	V_{CC} (2)	Input	Positive supply to the Stage 2 IF mixer.
36	I/P 2-	Input	Stage 2 mixer input @ 175.42MHz - inverse phase. One of a balanced input to the second stage IF mixer, to which one of the balanced signal outputs from the external 175MHz bandpass filter is connected.
37	I/P 2+	Input	Stage 2 mixer input @ 175.42MHz - true phase. Second of a balanced input to the second stage IF mixer, to which the second of the balanced signal outputs from the external 175MHz bandpass filter is connected.
38,39	V_{EE} (IF)	Input	Negative supply to the Stage 2 IF mixer, and Stage 3 IF block.
40	O/P 2-	Output	Stage 2 mixer output @ 35.42MHz - inverse phase. One of a balanced output from second stage IF mixer, to which one input of an external balanced 35.42MHz bandpass filter is connected. External dc biasing is required via an Inductor connected to V_{CC}. (See Note 3)
41	O/P 2+	Output	Stage 2 mixer output @ 35.42MHz - true phase. Second of a balanced output from second stage IF mixer, to which the second input of an external balanced 35.42MHz bandpass filter is connected. External dc biasing is required via an Inductor connected to V_{CC}. (See Note 3)
42	V_{CC} (3)	Input	Positive supply to the Stage 3 IF mixer.
43	I/P 3-	Input	Stage 3 mixer input @ 35.42MHz - inverse phase. One of a balanced input to the third stage IF mixer, to which one of the balanced signal outputs from the external 35.42MHz bandpass filter is connected. (See Note 3)
44	I/P 3+	Input	Stage 3 mixer input @ 35.42MHz - true phase. Second of a balanced input to the third stage IF mixer, to which the second of the balanced signal outputs from the external 35.42MHz bandpass filter is connected. (See Note 3)

Notes on Pin Descriptions

1). Both pins 4 & 6 (V_{EE} (OSC)) are connected internally, but must both be connected externally. If the VCO regulator is used (V_{CC} = +5.00V nominal) then pins 4 & 6 must be left floating with a 100nF capacitor to V_{CC}(OSC). In this configuration, the dc output level of the regulator can be monitored from V_{EE}(OSC), with respect to V_{CC}(OSC) - NOT 0V (V_{EE}/GND). For operation at V_{CC} <+4.0V, the VCO regulator cannot be used, and both V_{EE} (OSC) pins must be shorted to V_{EE} (REG) (Pin 7) - see Fig. 7.

2). The Digital Interface supply is independent from all the other supply pins, allowing supply separation to reduce the likelihood of undesirable digital signals interfering with the IF strip.

3). The 35.42MHz Bandpass filter should have a bandwidth of approx 2.0MHz. Ideally, this should be a DW9255 SAW filter.

CONTROL SIGNALS

	L	H
Power Down	Normal Operation	Powered Down
TEST	Normal Operation	Test

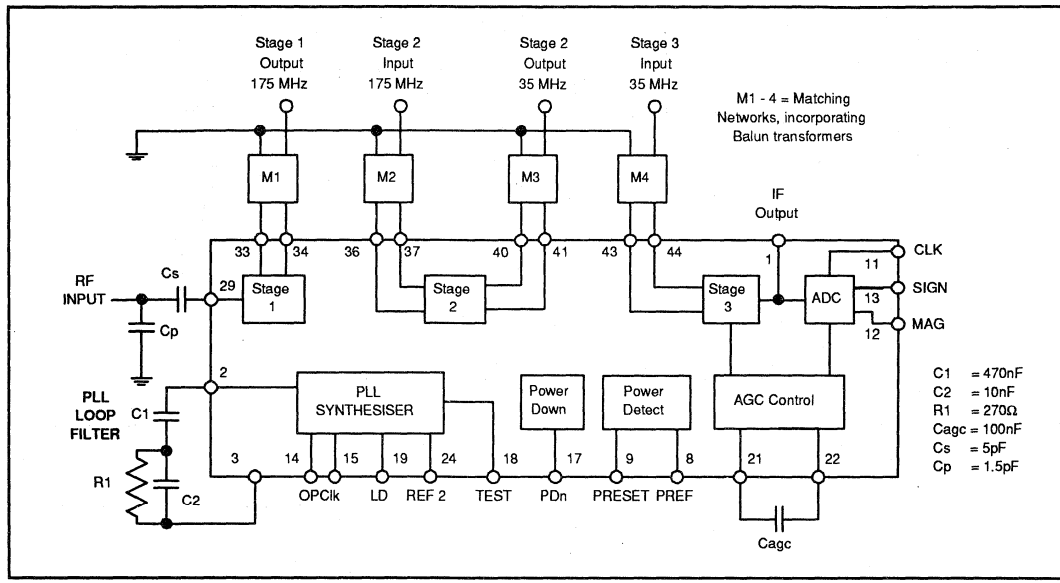


Fig. 3 GP2010 test circuit

OPERATING NOTES

A typical application circuit is shown in figure 4 with the GP2010 front-end interfaced to the GP2021 12 channel correlator integrated circuit. The RF input has an unmatched input impedance (see page 4). The RF input matching components Cs and Cp should be mounted as close to the RF input as possible: also the Vee(RF) tracks must be kept as short as possible. A SAW may be used as a 175.42MHz filter, but this can be replaced by a simpler coupled-tuned LC filter if there is no critical out-of band jamming immunity requirement. The DC bias to mixer 1 is provided via inductors L1 and L2, which may form part of the 175.42MHz filter. The output of mixer 2 requires an external dc bias, achieved with inductors L3 and L4, which also serve to tune out the input capacitance of the DW9255 SAW filter. The output of the SAW is tuned with inductor L5. The AGC capacitor (Cagc) determines the AGC time-constant. The PLL loop filter components are selected to give a PLL loop bandwidth of approx. 10kHz. The IF Output is normally used for test-purposes only, but is available to the user if required. In this configuration the device will operate with an input spectral noise density up to -130dBm/Hz, over the L1 C/A spread-spectrum bandwidth of 2 MHz. Typically a low noise preamplifier (gain >+15dB) is used, and may be located with a remote antenna.

QUALITY AND RELIABILITY

At GEC Plessey Semiconductors, quality and reliability are built into products by rigorous control of all processing operations, and by minimising random, uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures, recording of batch-by-batch data, using traceability procedures, and the provision of appropriate equipment and facilities to perform sample screening and conformance testing on finished product.

A common information management system is used to monitor the manufacturing on GEC Plessey Semiconductors CMOS and Bipolar processes. All products benefit from the use of an integrated monitoring system throughout all manufacturing operations, leading to high quality standards for all technologies.

Further information is contained in the Quality Brochure, available from GEC Plessey Semiconductors' Sales Offices.

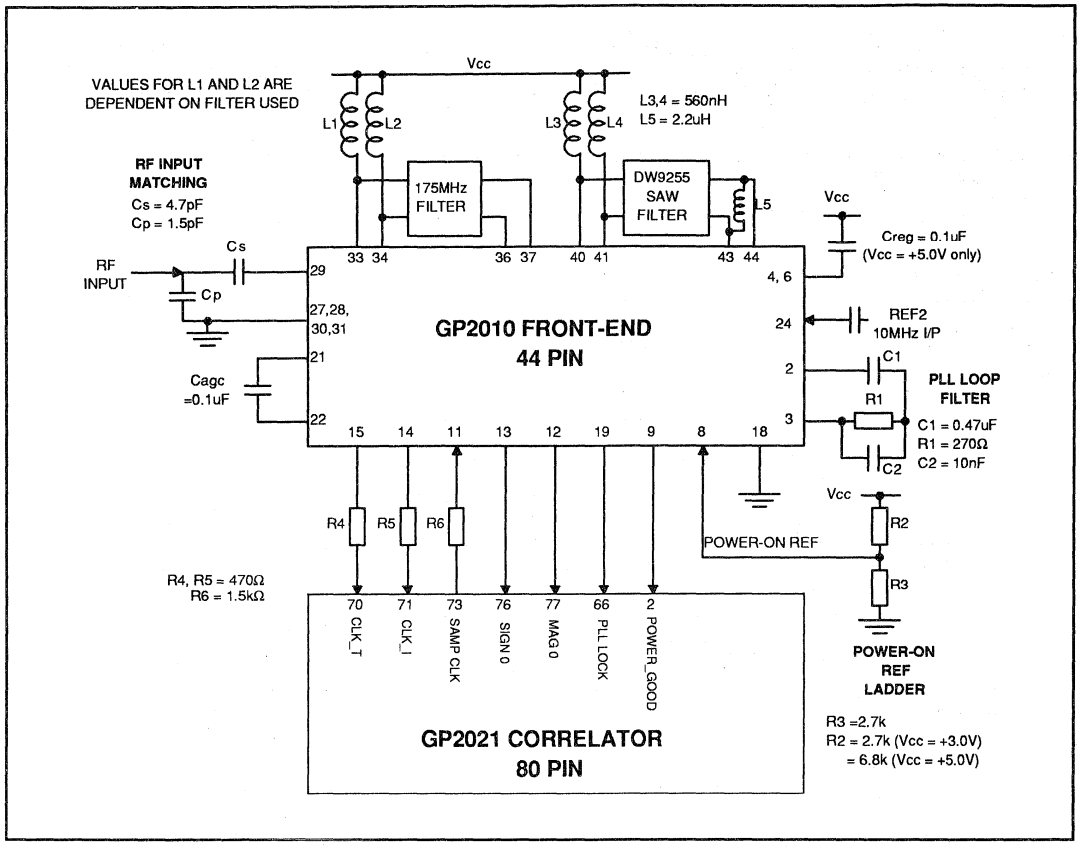


Fig. 4 GP2010 typical application

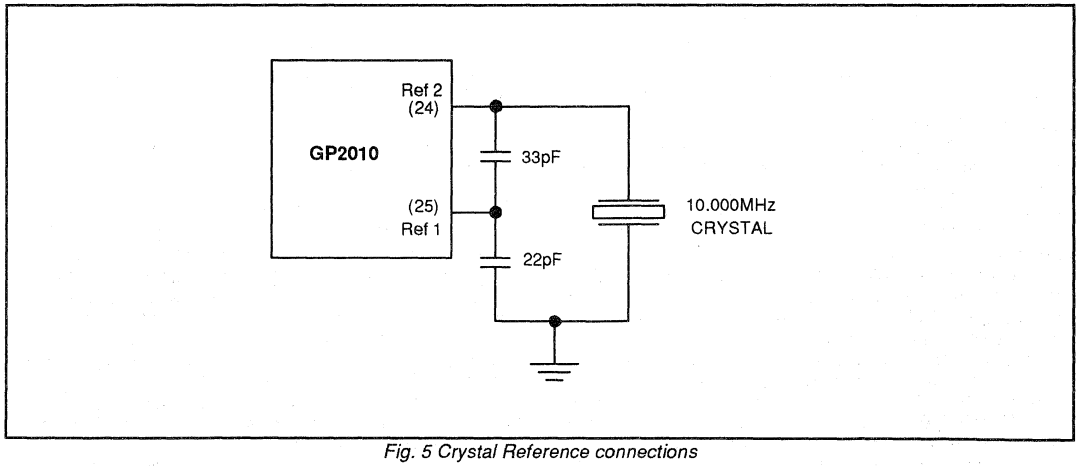


Fig. 5 Crystal Reference connections

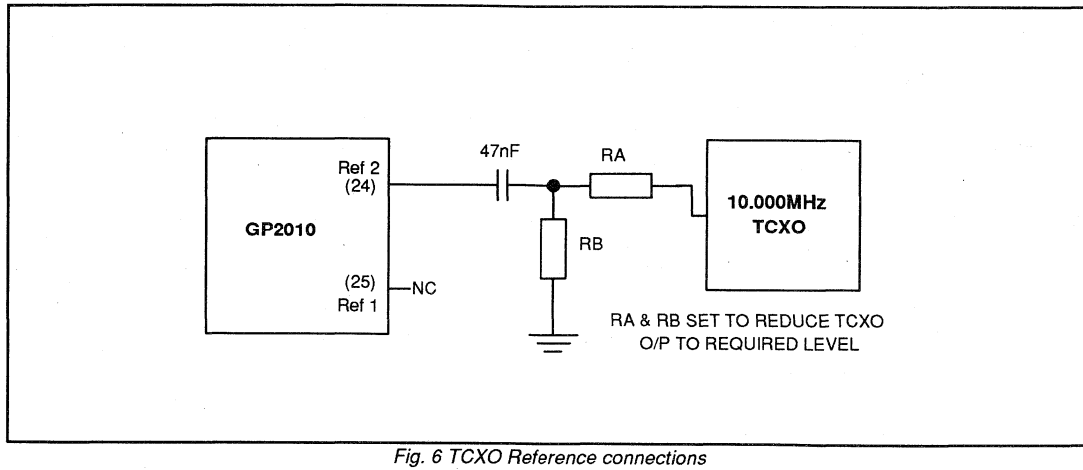


Fig. 6 TCXO Reference connections

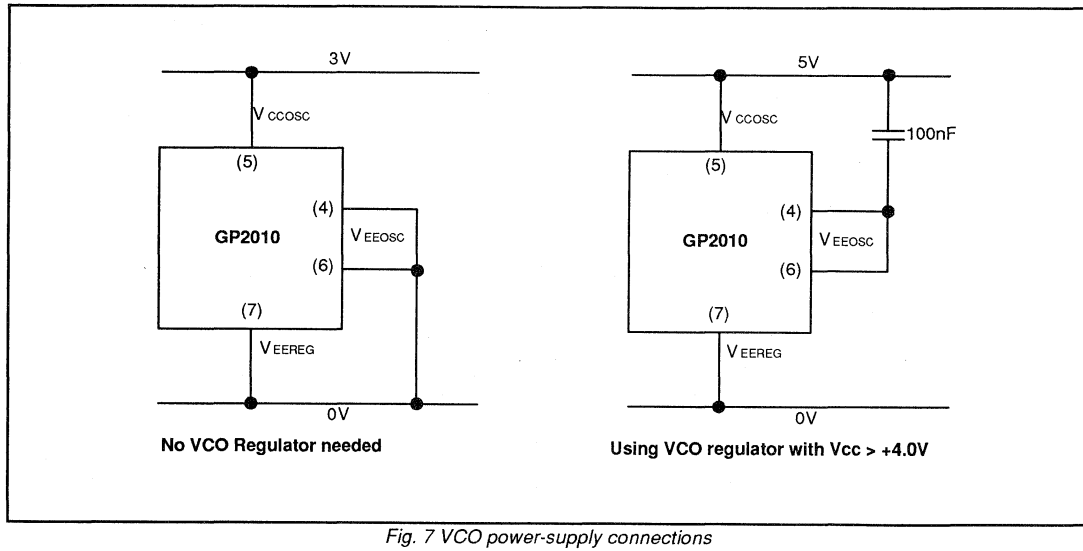


Fig. 7 VCO power-supply connections

GP2015

GLOBAL POSITIONING SYSTEM RECEIVER RF FRONT END

The GP2015 is a small format RF Front-end for Global Positioning System (GPS) receivers. Equivalent in performance to the GP2010 but in a TQFP package, this product is suited for size-critical applications as the RF area can be reduced by a factor of two to three using miniature surface mount passive components The GP2015 is designed to operate from either 3 or 5 Volt supplies.

The input to the device is the L1 (1575.42MHz) Coarse-Acquisition (C/A) code Global Positioning signal from an antenna (via a low-noise pre-amplifier). The output is 2-bit quantised for subsequent signal processing in the digital domain. The GP2015 contains an on-chip synthesiser, mixers, AGC and a quantiser which provides Sign and Magnitude digital outputs. A minimum of external components is required to make a complete GPS front-end.

The device has been designed to operate with the GP2021 12-channel Global Positioning Correlator, and DW9255 SAW filter, both also available from GEC Plessey Semiconductors.

FEATURES

- Ultra miniature TQFP package
- Low Voltage Operation (3V - 5V)
- Low Power - 200mW typ. (3V supply)
- C/A Code Compatible
- On-chip PLL Including Complete VCO
- Triple Conversion Receiver
- 48-Lead Surface Mount Quad Flat-Pack Package
- Sign and Magnitude Digital Outputs
- Compatible with GP2021 CMOS Correlator

APPLICATIONS

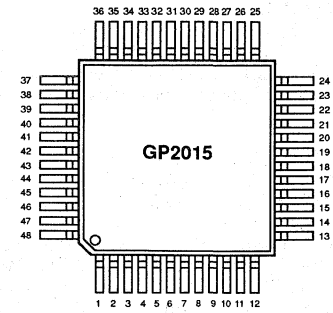
- C/A Code Global Positioning by Satellite Receivers
- Time Standards
- Navigation
- Surveying

ORDERING INFORMATION

The GP2015 is available in 48 pin TQFP package in Industrial (-40°C to +85°C) grade. The ordering code below is for standard screened devices.

ORDERING CODE

GP2015 IG FP1R Industrial - Plastic 48-pin TQFP



FP48

Pin	Name	Pin	Name
1	IF Output	25	N/C
2	PLL Filter 1	26	V_{CC} (DIG)
3	PLL Filter 2	27	REF 2
4	V_{EE} (OSC)	28	REF 1
5	V_{CC} (OSC)	29	V_{CC} (RF)
6	V_{EE} (OSC)	30	V_{EE} (RF)
7	V_{EE} (REG)	31	V_{EE} (RF)
8	PREF	32	RF Input
9	PRESET	33	V_{EE} (RF)
10	V_{EE} (IO)	34	V_{EE} (RF)
11	CLK	35	V_{CC} (RF)
12	N/C	36	N/C
13	N/C	37	O/P 1-
14	MAG	38	O/P 1+
15	SIGN	39	V_{CC} (2)
16	OPCIK-	40	I/P 2-
17	OPCIK+	41	I/P 2+
18	V_{DD} (IO)	42	V_{EE} (IF)
19	PD_N	43	V_{EE} (IF)
20	TEST	44	O/P 2-
21	LD	45	O/P 2+
22	V_{EE} (DIG)	46	V_{CC} (3)
23	AGC -	47	I/P 3-
24	AGC +	48	I/P 3+

Fig. 1 Pin connections - top view

RELATED PRODUCTS AND PUBLICATIONS

Part	Description	Data Reference
DW9255	35.42MHz SAW Filter	DS3861
GP2021	Twelve-Channel Correlator	DS4057
GPSBuilder	Twelve-Channel GPS receiver development system	DS4004
GP2010	GPS receiver RF Front-end	DS4056

ABSOLUTE MAXIMUM RATINGS (Non-simultaneous)

Max. Supply Voltage	7V
Max. RF Input	+15dBm
Max. voltage on any pin	V_{CC}/V_{DD} + 0.5V
except LD (pin 21) and PReset (pin 9), which are 5.5V	
Min. voltage on any pin	V_{EE} - 0.5V
Storage Temperature	-65°C to +150°C
Operation Junction Temperature	-40°C to +150°C
10MHz Reference Input	1.5V pk -pk

ESD PROTECTION

The GP2015 device is static sensitive. The most sensitive pins withstand a 750V test by the human body model. Therefore, ESD handling precautions are essential to avoid degradation of performance or permanent damage to this device.

PRODUCT DESCRIPTION

The GP2015 is a complete front-end down-converter for Global Positioning System (GPS) receivers. It is a state-of-the-art design combining an on-chip PLL synthesiser at 1400MHz, a low-noise amplifier, 3 mixers, and a 2-bit A to D converter. The GP2015 receives the 1575.42MHz signal transmitted by GPS satellites and converts it to a 4.309MHz IF, using triple down-conversion. The 4.309MHz IF is sampled to produce a 2-bit digital output. If the GP2015 is used in conjunction with the GP2021 correlator, then the GP2021 provides a sampling clock of 5.714MHz. This converts the IF to a 1.405MHz 2-bit digital output at TTL levels.

The GP2015 can operate from a single supply from +3V (nominal) to +5V (nominal).

A block diagram of the circuit is shown in figure 2.

IF STRIP

The input signal to the GP2015 is the GPS L1 signal received via an antenna and a suitable LNA. The L1 input is a spread spectrum signal at 1575.42MHz with 1.023Mbps BPSK modulation. The signal level at the antenna is about -130dBm, spread over a 2.046MHz bandwidth, so the wanted signal is actually buried in noise. The high RF input compression point of the GP2015 means that with subsequent IF filtering it is possible to reject large out of band jamming signals, in particular 900MHz as used by mobile telephones. The on-chip PLL generates the first local-oscillator frequency at 1400MHz. The output of the front-end mixer (Stage 1) at 175.42 MHz can then be filtered before being applied to the second stage. The double-balanced stage 1 mixer outputs are open-collectors, and require external dc bias to V_{CC}.

The second stage contains further gain and a mixer with a local oscillator signal at 140 MHz giving a second IF at 35.42 MHz. The second stage mixer is also double-balanced with open-collector outputs requiring external dc bias to V_{CC}.

The signal from stage 2 is passed through an external filter with a 1dB bandwidth of 1.9MHz. The performance of this filter is critical to system performance and it is recommended that a SAW filter is used (part number DW9255, also available from GEC Plessey Semiconductors). The output of the filter then feeds the main IF amplifier. This includes 2 AGC amplifiers and a third mixer with a local oscillator signal at 31.111 MHz giving a final IF at 4.309 MHz. There is an on-chip filter after the third mixer which provides filtering centred on 4.309 MHz. The IF output, which has 1kΩ output impedance, is provided for test purposes. All of the signals within the IF amplifier are differential including the filter inputs and outputs, except the IF output (pin 1), to reduce any common mode interference.

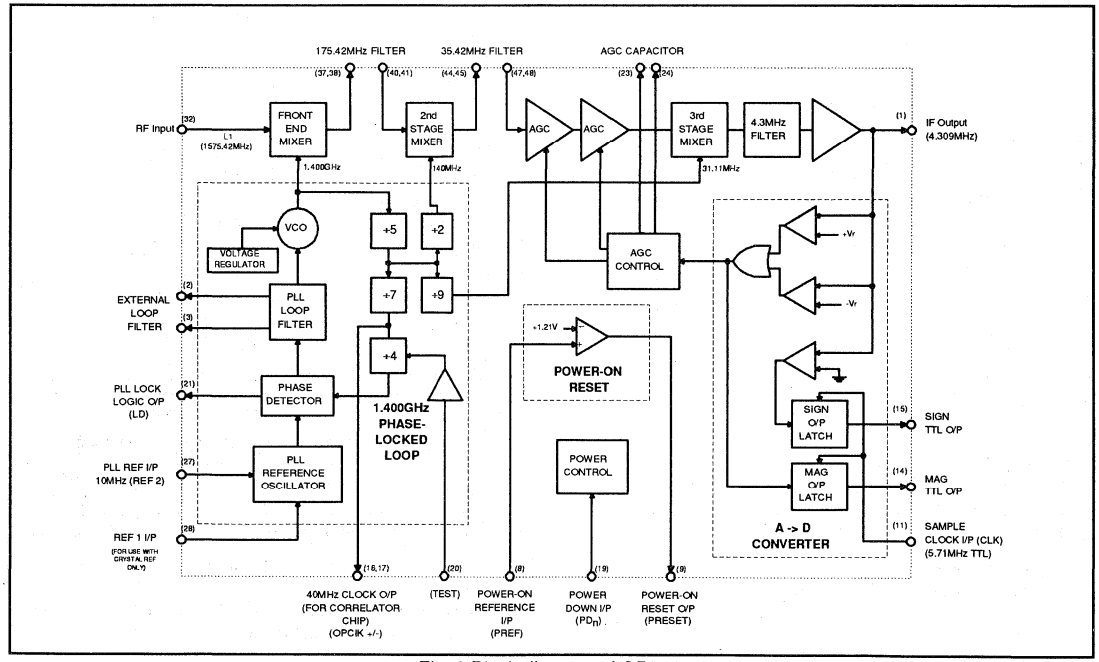


Fig. 2 Block diagram of GP2015

The IF output is fed to a 2-bit quantiser which provides sign and magnitude (MSB and LSB) outputs. The magnitude data controls the AGC loop, such that on average the magnitude bit is set (high) 30% of the time. The AGC time constant is set by an external capacitor.

The sign and magnitude data, SIGN (pin 15) and MAG (pin 14), are latched by the rising edge of the sample clock, CLK (pin 11), which is normally derived from the correlator; the GP2021 provides a 5.714MHz (=40/7) clock, giving a sampled IF centred on 1.405MHz.

The Digital Interface circuits use a separate power-supply, V_{DD}(IO), which would normally be shared with the correlator to minimise crosstalk between the analog and digital sections of the device.

ON-CHIP PHASE-LOCKED LOOP SYNTHESISER

All of the local oscillator signals are derived from an on chip phase locked loop synthesiser. This includes a 1400MHz VCO complete with on-chip tank circuit, dividers and phase detector, with external loop filter components. A 10.000MHz reference frequency is required for the PLL. This can be achieved by attaching an external 10.000MHz crystal to the on-chip PLL reference oscillator (see figure 5). However in most applications the user will need an external source, such as a TCXO, to provide greater frequency stability (see figure 6). An external reference should be ac coupled to REF2 (pin 27); REF 1 (pin 28) should be left open circuit.

The three local oscillator signals 1400MHz, 140.0MHz and 31.11MHz are derived from the 1400MHz synthesiser output. The synthesiser also provides a 40 MHz balanced differential output clock (pins 16 & 17) which can be used to clock the GP2021 correlator. The clock is a low level differential signal which helps minimise interference with the analog areas of the circuit. A PLL lock-detect output, LD (pin 21), is also provided, which is logic high when the PLL is phase-locked to the 10.000MHz reference signal.

The VCO power-supply incorporates an on-chip regulator to improve the noise-immunity of the PLL. This feature is only available when operating with a 5 volt (nominal) supply which is regulated to 3.3 volts internally. This internal regulated supply is referenced to V_{CC}(OSC) (pin 5). Figure 7 shows the required connections for both 3 volt and 5 volt operation.

A further feature of the circuit is the TEST input (pin 20). When this input is held high the PLL is unlocked with the VCO at its maximum frequency.

POWER-DOWN CAPABILITY

A power down function is provided on the GP2015, to limit power consumption. This powers down the majority of the circuit except the "power-on reset" function (see below).

If the power down feature is not required, the Power-down input, PD_n (pin 19), should be connected to 0V dc (=Vee/Ground).

POWER-ON RESET FUNCTION

The GP2015 includes a voltage detector which operates from the digital interface supply. This circuit is used to produce a TTL logic low output while the GPS receiver power supply is switching on, and produces a logic high output when the power supply voltage has achieved a nominal value. This output can be used to disable the GP2021 correlator while the power supply is switching on. An internal bandgap reference of approximately +1.21V is compared with the voltage on a sense pin, PREF (pin 8); when the voltage on this pin exceeds the reference, a TTL logic high level appears at the Power-on Reset output, PRESET (pin 9). Thus, if the sense input voltage is derived from an external resistive divider from the Digital Interface supply, V_{DD}(IO) (pin 16), such that the sense voltage at nominal V_{CC} is V_S, then the supply threshold, Vcc(thresh), at which the PRESET output goes to logic high is:-

$$V_S = \frac{V_{CC}\ (nom) \times 1.21}{V_{CC}\ (thresh)}$$

For a V_{CC} (nom) of 5.0V, V_{CC} (thresh) may be set to approx. 4.0V, giving V_S of 1.5V.

For a V_{CC} (nom) of 3.0V, V_{CC} (thresh) may be set to approx. 2.4V, giving V_S of 1.5V.

ADDITIONAL INFORMATION

All the digital inputs and outputs can use a separate power supply to help prevent digital switching transitions interacting with the analog sections of the device, and as an additional precaution, the digital inputs and outputs are on the opposite side of the device to the critical analog pins.

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions (see Fig. 3 for test circuit):

Industrial (I) grade: T_{AMB} = -40°C to +85°C
Supply voltage: V_{CC} and V_{DD} = +2.7V to +5.5V

Test conditions (unless otherwise stated):

Supply voltages: V_{CC} = +2.7V and +5.5V, V_{DD} = +2.7V and +5.5V
Test temperature: Industrial (I) grade product: +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
SUPPLY CURRENT					
Normal mode - Analog interface		55	77	mA	Pins 5, 26, 29, 35, 39, 46
- Digital interface		9	14.5	mA	Pin 18
Power down mode - Analog interface		3	6	mA	Pins 5, 26, 29, 35, 39, 46
- Digital interface		3	5	mA	Pin 18
Power Supply Differential			100	mV	Between any V_{CC}/V_{DD} pins (Note 7)
Power down Response time		3		µs	(Note 7)
IF STRIP					
Front End/Mixer 1					
Conversion Gain (G1)	11	18	25	dB	R_O = 600Ω (Note 2)
					F_{IN} = 1575.42MHz
Noise Figure		9		dB	Z_S = 50Ω (Note 7)
Input Compression (1dB)	-22	-16		dBm	
Input Impedance		17		Ω	Pin 32 (Notes 1 and 7)
		3.4		nH	(Notes 1 and 7)
Differential Output Impedance		700		Ω	Pins 37 & 38 (Note 8)
RF Input Image Rejection		7		dB	F_{IN} = 1224.58MHz (Note 7)
Stage 2/Mixer 2					
Conversion Gain (G2)	22	27	33	dB	F_{IN} = 175.42MHz
Input Compression (1dB)	5	14		mV rms	
Differential Input Impedance		700		Ω	Pins 40 & 41 (Note 8)
Differential Output Impedance		500		Ω	Pins 44 & 45 (Note 8)
Stage 3					
High Gain (In terms of total strip)	106-G1-G2			dB	(Note 6)
High Gain (G3)		75		dB	F_{IN} = 35.42MHz
Gain Control Range		60		dB	(Note 3)
Differential Input Impedance		1		kΩ	Pins 47 & 48 (Note 8)
IF Output amplitude	60	85	120	mV rms	CW input (Note 3)
IF Output impedance		1		kΩ	Pin 1(Note 8)
4.3MHz Filter Response					
Flatness 4.3 ± 1MHz	-1.5		+1.0	dB	
Rejection @ 0.5MHz		14		dB	(Note 7 and 9)
@ 50MHz	45	70		dB	
2 BIT QUANTISER					
Sign Duty Cycle	40	50	60	%	} (Note 10)
Mag Duty Cycle	20	30	40	%	
AGC Time Constant		2		ms	C_{AGC} = 100nF
ON_CHIP PLL SYNTHESISER					
Phase Noise					15kHz Loop Bandwidth
± 1kHz		-68		dBc/Hz	} (Note 7)
± 10kHz		-75		dBc/Hz	
± 100kHz		-88		dBc/Hz	
± 1MHz		-110		dBc/Hz	
± 5MHZ		-120		dBc/Hz	
± 50MHz		-120		dBc/Hz	
PLL Spurs		-50		dBc	(Note 7)

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
VCO Maximum Lock Frequency	1414			MHz	
VCO Minimum Lock Frequency			1386	MHz	
VCO regulator output voltage	3	3.3	3.5	V	(Note 4)
VCO Gain	50	150	240	MHz/V	
Phase Detector Gain		5.3		V/rad	(Note 7)
10MHz Reference Input	0.1	0.6	1.2	V pk-pk	Pin 27
10MHz Reference Input Impedance		5		kΩ	(Note 11)
PLL Lockup Time		6		ms	From Power up (Note 7)
PLL Loop Gain		150		dB	(Note 7)
DIGITAL INTERFACES					
Sample Clock, Power Down, Test Inputs.					Pins 11, 19, 20
V_{IH}	2		V_{DD}	V	
V_{IL}	0		0.5	V	
Input Current High I_{IH}			10	µA	$V_{IH} = V_{DD}$
Input Current Low I_{IL}	-300			µA	$V_{IL} = V_{EE}$
Sign/Mag Outputs					Pins 15, 14
V_{OH}	V_{DD}-1			V	I_O = -0.5mA
V_{OL}			0.5	V	I_O = 0.5mA
Sample Clock to Sign/Mag Delay		20		ns	CL = 15pF, RL = 15kΩ (Note 7)
40MHz Clock Output					
High Level (V_{OH})	V_{DD}-1.25	V_{DD}-1	V_{DD}-0.8	V	Pins 16 & 17
Low Level (V_{OL})		V_{OH}-0.1		V	(Note 5)
Output (differential)		220		mV p-p	CL = 15pF (GND) (Note 7)
					CL = 5pF (Diff) (Note 7)
Duty Cycle		43		%	(Note 7)
LD (PLL Lock)/PRESET Outputs					Pins 21 and 9
Low Level (V_{OL})		0.2	0.5	V	I_O = 0.5mA
High Level (V_{OH})	V_{DD}-1	V_{DD}		V	I_O = -10µA
Power-on reset comparator input					Pin 8
Power Reset Threshold Level	1.1	1.21	1.35	V	
Power Reset Reference Input Current	-10		10	µA	

Notes On Electrical Characteristics:- All RF measurements are made with appropriate matching to the input or output impedances, such as balun transformers, and levels refer to matched 50ohm ports (see figure 3 for test circuit)

1. RF input impedance (series) without input matching components connected - expressed as Real impedance with reactive inductor value.
2. Input matched to 50ohm, output loaded with 600ohm differential
3. Maximum Stage 3 input signal amplitude for correct AGC operation = 20mV rms.
4. VCO regulator voltage measured with respect to Vcc (OSC) - pin 5.
5. The OPCLK outputs are differential and are referenced to V_{DD}.
6. Minimum gain requirement expressions:

$$-7dBm < -174dBm/Hz + 19dB + G1 + G2 + G3 - 21dB + 63dB$$

where -7dBm = typical IF Output level with AGC active (equivalent to 100mV rms)
-174dBm/Hz = background noise level at RF input
19dB = sum of LNA gain and noise figure
-21dB = total loss in 175MHz and 35MHz filters
63dB = summation of noise over a 2MHz bandwidth

Rearranging the above expression gives G1 + G2 + G3 > 106dB.

7. This parameter is not production tested.
8. This impedance is toleranced at +/-30% and is not production tested.
9. Roll off occurs in on-chip capacitive coupling IF Output to input of ADC circuit. Not measurable at IF Output.
10. CW input on pins 47 & 48 of 35.42MHz at 7mV rms.
11. This input impedance applies to the typical input level. The impedance is level dependent and is not tested or guaranteed.

PIN DESCRIPTIONS

All V_{EE} and V_{CC}/V_{DD} pins must be connected to ensure correct operation

Pin No.	Signal Name	Input/Output	Description
1	IFOutput	Output	IF Test output. Connected to output of Stage 3 prior to the A to D converter. A series 1kΩ resistor is incorporated for buffering purposes.
2	PLL Filter 1	Output	PLL Filter 1. Connected to the bias network within the on-chip VCO. An external PLL loop filter network should be connected between this pin and PLL Filt 2 (see below).
3	PLL Filter 2	Output	PLL Filter 2. Connected to the varactor diodes within the on-chip VCO. An external PLL loop filter network should be connected between this pin and PLL Filt 1 (see above).
4,6	V_{EE} (OSC)	Input	Negative supply to the on-chip VCO. (See Note 1)
5	V_{CC} (OSC)	Input	Positive supply to the on-chip VCO.
7	V_{EE} (REG)	Input	Negative supply to the VCO regulator. This must be connected to GND.
8	PREF	Input	Power-on Reset Reference input. An on-chip comparator produces a logic HI when the PRef input voltage exceeds +1.21V.
9	PRESET	Output	Power-on Reset Output. A TTL compatible output controlled by the Power-on reset comparator (See above). This output remains active even when the chip is powered down. (See pin 19 - PDn).
10	V_{EE} (IO)	Input	Negative supply to the Digital Interface. (See Note 2)
11	CLK	Input	Sample Clock input from the correlator chip. A TTL compatible input (which operates at 5.714MHz if used with GP2021 correlator device) used to clock the MAG & SIGN output latches, on the **rising** edge of the CLK signal.
12, 13	N/C		Not connected. (See Note 4)
14	MAG	Output	Magnitude bit data output. A TTL compatible signal, representing the *magnitude* of the mixed down IF signal. Derived from the on-chip 2-bit A to D converter, synchronised to the CLK input clock signal.
15	SIGN	Output	Sign bit data output. A TTL compatible signal, representing the *polarity* of the mixed down IF signal. Derived from the on-chip 2-bit A to D converter, synchronised to the CLK input clock signal.
16	OPClk-	Output	40MHz Clock output - inverse phase. One side of a balanced differential output clock, with opposite polarity to Pin 17 - OPClk+. Used to drive a master-clock signal within the correlator chip.
17	OPClk+	Output	40MHz Clock output - true phase. Other side of a balanced differential output clock set, with opposite polarity to Pin 16 - OPClk-. Used to drive a master-clock signal within the correlator chip.

Pin No.	Signal Name	Input/Output	Description
18	V_{DD} (IO)	Input	Positive supply to the Digital Interface. (See Note 2)
19	PDn	Input	Power-Down control input. A TTL compatible input, which when set to logic high, will disable ALL of the GP2015 functions, except the power-on reset block. Useful to reduce the total power consumption of the GP2015. If this feature is not required, the pin should be connected to 0V (V_{EE}/GND).
20	TEST	Input	Test control input - Disable PLL. A TTL compatible input, which when set to logic high, will disable the on-chip PLL, by disconnecting the divided-down VCO signal to the phase-detector. The VCO will free run at its upper range of frequency operation. If this feature is not required, the pin should be connected to 0V (V_{EE}/GND).
21	LD	Output	PLL Lock Detect output. A TTL compatible output, which indicates if the PLL is phase-locked to the PLL reference oscillator. Will become logic high only when phase-lock is achieved.
22	V_{EE} (DIG)	Input	Negative supply to the PLL and A to D converter.
23	AGC-	Output	AGC Capacitor output - inverse phase. One side of a balanced output from the AGC block within IF Stage 3, to which an external capacitor is connected to set the AGC time-constant.
24	AGC+	Output	AGC Capacitor output - true phase. One side of a balanced output from the AGC block within IF Stage 3, to which an external capacitor is connected to set the AGC time-constant.
25	N/C		Not connected. (See Note 4)
26	V_{CC} (DIG)	Input	Positive supply to the PLL and A to D converter.
27	REF 2	Input	10.000MHz PLL Reference signal input . Input to which an externally generated 10.000MHz PLL reference signal should be ac coupled, if an external PLL reference frequency source (e.g TCXO) is used (see fig. 6). If no external reference is used, this pin forms part of the on-chip PLL reference oscillator, in conjunction with an external 10.000MHz crystal (see fig. 5).
28	REF 1	Input	PLL reference oscillator auxillary connection. Used in conjunction with Pin 27 (REF 2) to allow a 10.000MHz external crystal to provide the PLL reference signal if no external PLL reference frequency source (e.g TCXO) is used. This pin should NOT be connected if an external TCXO is being used (see fig. 5).
29, 35	V_{CC} (RF)	Input	Positive supply to the RF input and Stage 1 IF mixer. Both pins are connected internally, but must both be connected to V_{CC} externally, to keep series inductance to a minimum.
30, 31, 33, 34	V_{EE} (RF)	Input	Negative supply to the RF input and Stage 1 IF mixer. The pins are all connected internally, but must ALL be connected to 0V (V_{EE}/GND) externally, to keep series inductance to a minimum.

Pin No.	Signal Name	Input/Output	Description
32	RF Input	Input	RF input. The GPS RF input signal @ 1575.42MHz from an external antenna with LNA and filter is connected to this pin via an input-matching network (see fig.4).
36	N/C		Not connected. (See Note 4)
37	O/P 1-	Output	Stage 1 mixer output @ 175.42MHz - inverse phase. One of a balanced output from first stage IF mixer, to which one input of an external balanced 175MHz bandpass filter is connected. External dc biasing is required via an inductor connected to V_{CC}(RF) - the value of which is dependent on the filter used.
38	O/P 1+	Output	Stage 1 mixer output @ 175.42MHz - true phase. Second of a balanced output from first stage IF mixer, to which the second input of an external balanced 175MHz bandpass filter is connected. External dc biasing is required via an inductor connected to V_{CC}(RF) - the value of which is dependent on the filter used.
39	V_{CC} (2)	Input	Positive supply to the Stage 2 IF mixer.
40	I/P 2-	Input	Stage 2 mixer input @ 175.42MHz - inverse phase. One of a balanced input to the second stage IF mixer, to which one of the balanced signal outputs from the external 175MHz bandpass filter is connected.
41	I/P 2+	Input	Stage 2 mixer input @ 175.42MHz - true phase. Second of a balanced input to the second stage IF mixer, to which the second of the balanced signal outputs from the external 175MHz bandpass filter is connected.
42, 43	V_{EE} (IF)	Input	Negative supply to the Stage 2 IF mixer, and Stage 3 IF block.
44	O/P 2-	Output	Stage 2 mixer output @ 35.42MHz - inverse phase. One of a balanced output from second stage IF mixer, to which one input of an external balanced 35.42MHz bandpass filter is connected. External dc biasing is required via an Inductor connected to V_{CC}. (See Note 3)
45	O/P 2+	Output	Stage 2 mixer output @ 35.42MHz - true phase. Second of a balanced output from second stage IF mixer, to which the second input of an external balanced 35.42MHz bandpass filter is connected. External dc biasing is required via an Inductor connected to V_{CC}. (See Note 3)
46	V_{CC} (3)	Input	Positive supply to the Stage 3 IF mixer.
47	I/P 3-	Input	Stage 3 mixer input @ 35.42MHz - inverse phase. One of a balanced input to the third stage IF mixer, to which one of the balanced signal outputs from the external 35.42MHz bandpass filter is connected. (See Note 3)
48	I/P 3+	Input	Stage 3 mixer input @ 35.42MHz - true phase. Second of a balanced input to the third stage IF mixer, to which the second of the balanced signal outputs from the external 35.42MHz bandpass filter is connected. (See Note 3)

Notes on Pin Descriptions

1). Both pins 4 & 6 (V_{EE} (OSC)) are connected internally, but must both be connected externally. If the VCO regulator is used (V_{CC} = +5.00V nominal) then pins 4 & 6 must be left floating with a 100nF capacitor to V_{CC}(OSC). In this configuration, the dc output level of the regulator can be monitored from V_{EE}(OSC), with respect to V_{CC}(OSC) - NOT 0V (V_{EE}/GND). For operation at V_{CC} <+4.0V, the VCO regulator cannot be used, and both V_{EE} (OSC) pins must be shorted to V_{EE} (REG) (Pin 7) - see Fig. 7.

2). The Digital Interface supply is independent from all the other supply pins, allowing supply separation to reduce the likelihood of undesirable digital signals interfering with the IF strip.

3). The 35.42MHz Bandpass filter should have a bandwidth of approx 2.0MHz. Ideally, this should be a DW9255 SAW filter.

4). These pins are not connected within the package, and may therefore be used in power/ground routing if desired. To avoid crosstalk, their use in signal routing is not recommended.

CONTROL SIGNALS

	L	H
Power Down	Normal Operation	Powered Down
TEST	Normal Operation	Test

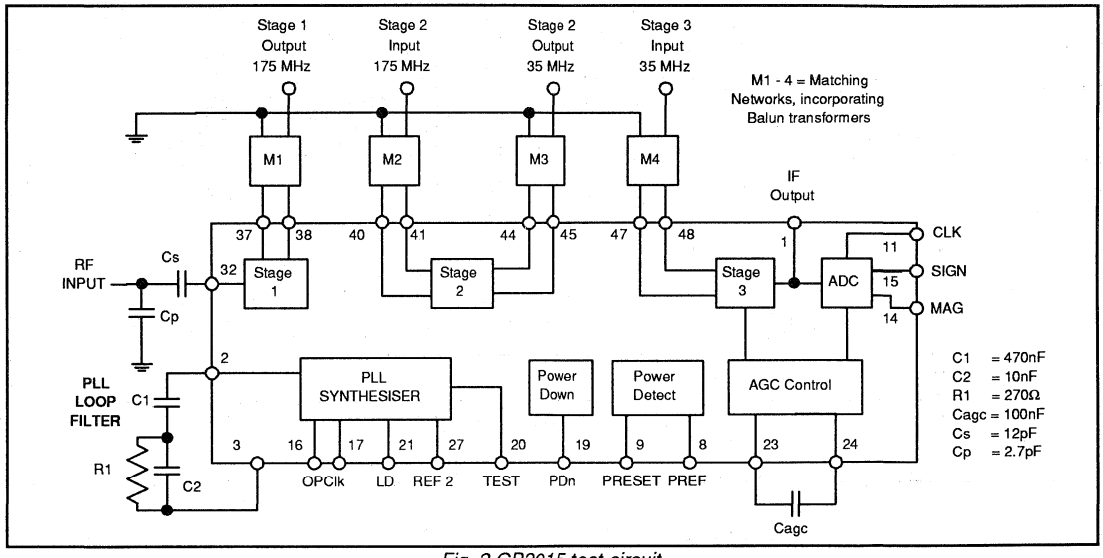


Fig. 3 GP2015 test circuit

OPERATING NOTES

A typical application circuit is shown in figure 4 with the GP2015 front-end interfaced to the GP2021 12-channel correlator integrated circuit. The RF input has an unmatched input impedance (see page 4). The RF input matching components Cs and Cp should be mounted as close to the RF input as possible: also the Vee(RF) tracks must be kept as short as possible. A SAW filter may be used as a 175.42MHz filter, but this can be replaced by a simpler coupled-tuned LC filter if there is no critical out-of-band jamming immunity requirement. The DC bias to mixer 1 is provided via inductors L1 and L2, which may form part of the 175.42MHz filter. The output of mixer 2 requires an external dc bias, achieved with inductors L3 and L4, which also serve to tune out the input capacitance of the DW9255 SAW filter. The output of the SAW filter is tuned with inductor L5. Capacitor (Cagc) determines the AGC time-constant. The PLL loop filter components are selected to give a PLL loop bandwidth of approximately 10kHz. The IF Output is normally used for test-purposes only, but is available to the user if required. Typically a low noise preamplifier (gain >+15dB) is used between the antenna and the RF input (pin 32), and may be located remotely, with the antenna.

QUALITY AND RELIABILITY

At GEC Plessey Semiconductors, quality and reliability are built into products by rigorous control of all processing operations, and by minimising random, uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures, recording of batch-by-batch data, and the use of traceability procedures.

A common information management system is used to monitor the manufacturing on GEC Plessey Semiconductors CMOS and Bipolar processes. All products benefit from the use of an integrated monitoring system throughout all manufacturing operations, leading to high quality standards for all technologies.

Further information is contained in the Quality Brochure, available from GEC Plessey Semiconductors' Sales Offices.

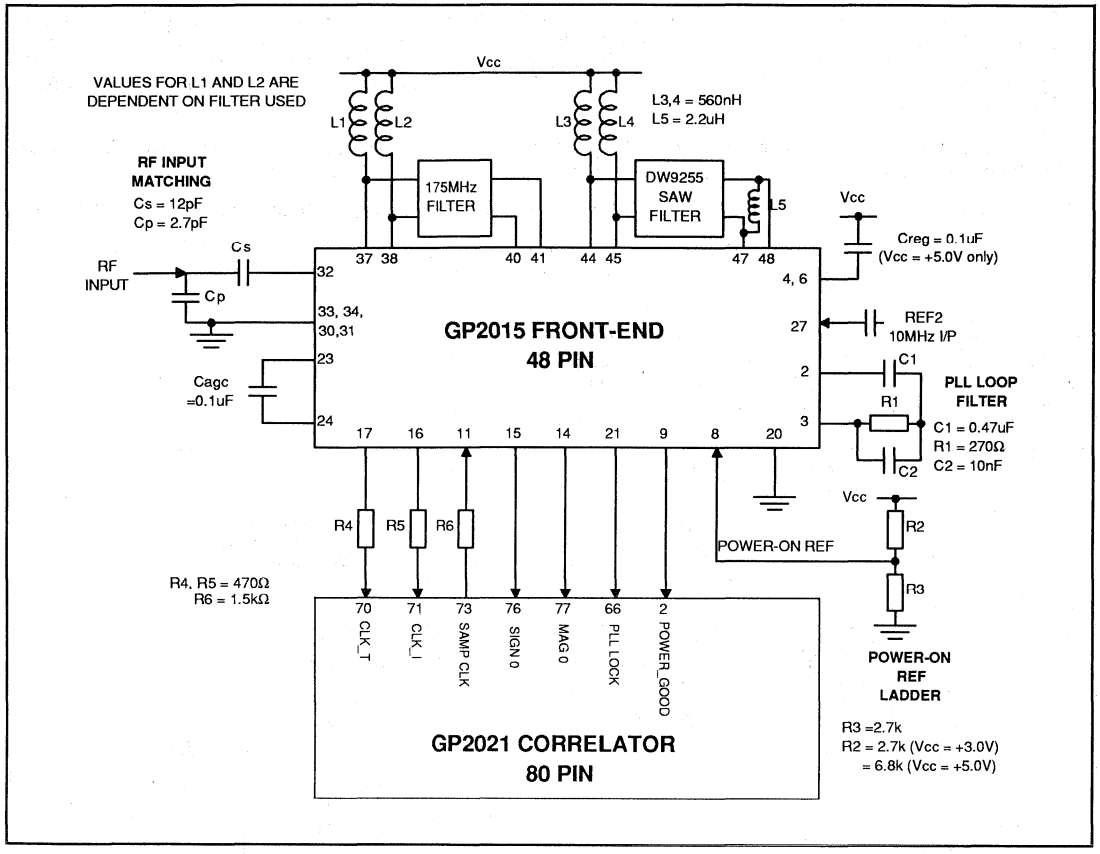


Fig. 4 GP2015 typical application

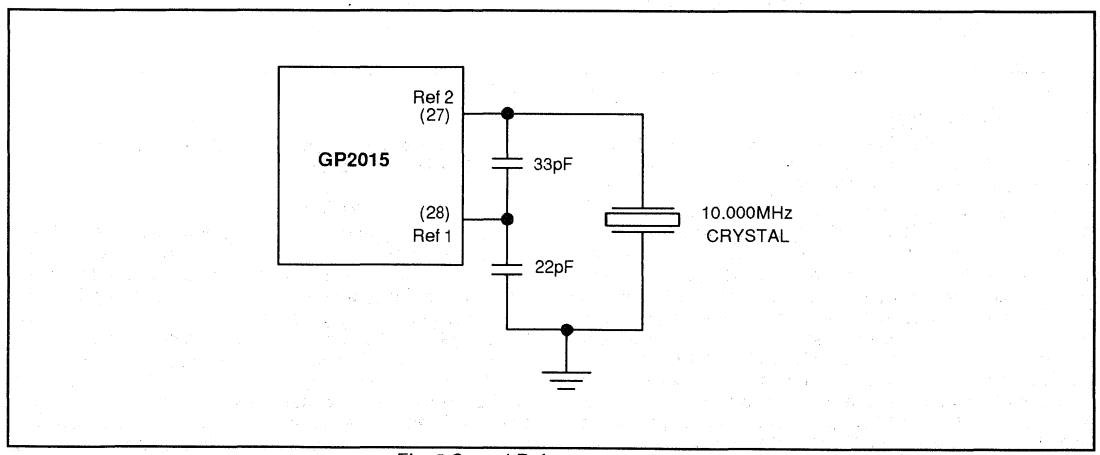


Fig. 5 Crystal Reference connections

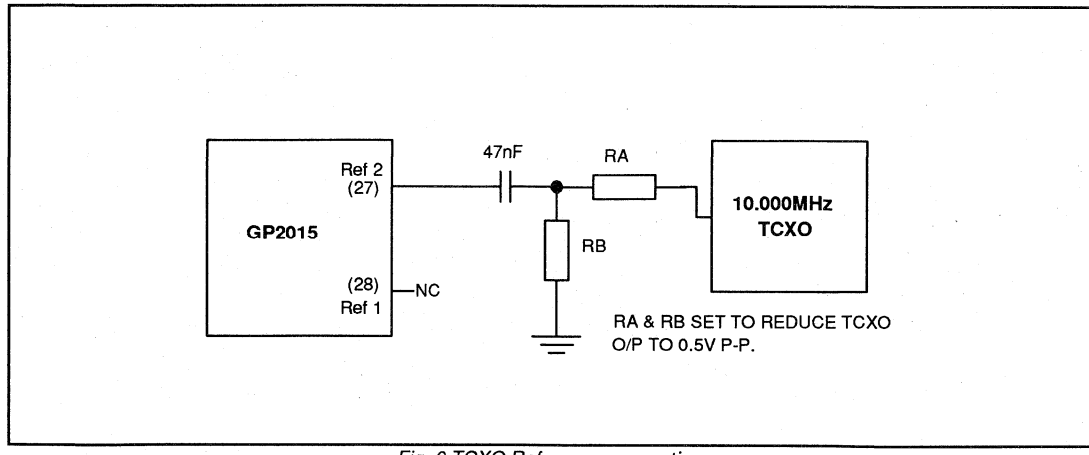


Fig. 6 TCXO Reference connections

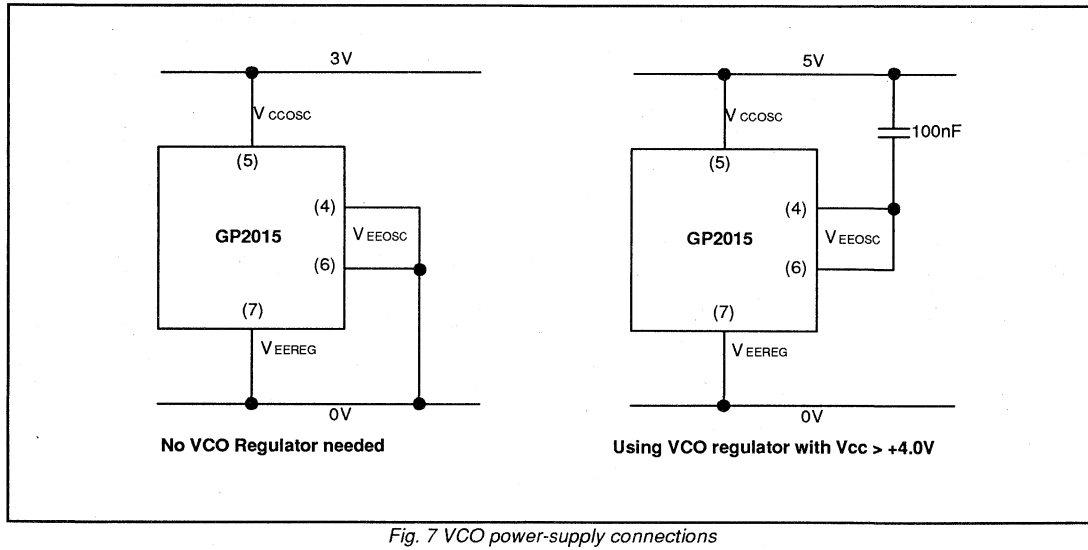


Fig. 7 VCO power-supply connections

DW9255

35.42MHz SAW FILTER FOR GLOBAL POSITIONING SYSTEM RECEIVERS

The DW9255 is a Surface Acoustic Wave (SAW) bandpass filter for use with the GP2000 Global Positioning System (GPS) receiver chip-set, available from GEC Plessey Semiconductors. It is pre-tuned to the exact 2nd IF filter requirements of the GP2010 & GP2015 RF front-end devices, with a centre-frequency of 35.42MHz. The response is tuned for a flat passband, steep stopband and uniform passband group-delay with 3 external inductors. The device is realised on a Lithium Tantalate substrate and housed in a small leadless ceramic Surface Mount package.

The DW9255 gives significant improvement in correlated GPS Signal-to-Noise Ratio (SNR) performance compared to conventional LC bandpass filter schemes. This aids satellite signal acquisition and tracking capability from the GP2000 GPS chip-set. This device effectively filters out-of-band (unwanted) noise in the GPS signal. The Automatic Gain Control (AGC) within the GP2010 and GP2015 RF Front-end devices will then operate only on in-band noise for optimum gain and superior correlated GPS signal strength.

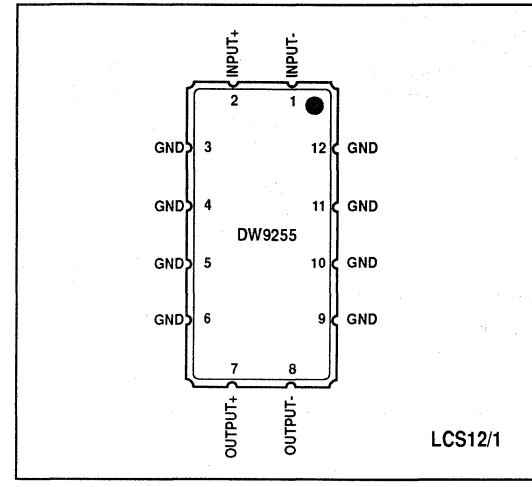


Fig.1 Pinout

FEATURES

- Centre Frequency of 35.42MHz
- Insertion Loss of 17dB ±1dB (typical)
- 1dB Bandwidth 1.9MHz (typical)
- Passband Ripple 0.8dB (typical)
- Low Profile Ceramic Surface Mount Package
- Operating Temperature Range -40° to +85°C

APPLICATION

- Commercial Global Positioning

RELATED PRODUCTS AND PUBLICATIONS

Part	Description	Data Reference
GP2010	GPS receiver RF Front-end	DS4056
GP2015	Miniature GPS receiver RF Front-end	DS4374

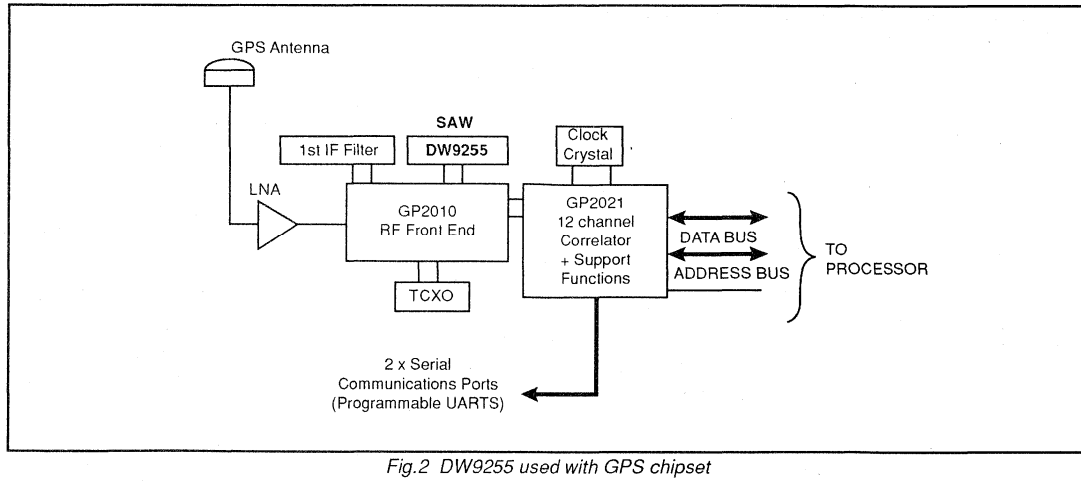


Fig.2 DW9255 used with GPS chipset

ELECTRICAL CHARACTERISTICS (Typ. @ 25°C)

Parameter		Min	Typ	Max	Units
Centre Frequency		-	35.42	-	MHz
1dB Bandwidth		1.6	1.9	-	MHz
Insertion Loss		16	17	18	dB
Amplitude Ripple (34.62 to 36.22MHz)		-	0.8	1.6	dB (pk to pk)
Relative Attenuation	<28MHz	35	40	-	dB
(relative to insertion loss)	<31MHz	30	35	-	dB
	<33.5MHz	21	25	-	dB
	>37.5MHz	21	25	-	dB
	>40MHz	25	30	-	dB
	>50MHz	30	40	-	dB
	>63MHz	28	35	-	dB
	>73 - 110MHz	40	45	-	dB
Group Delay Ripple (34.62 to 36.22MHz)		-	190	300	ns
Maximum Group Delay (34.62 to 36.22MHz)		-	1.6	1.7	µs
Operating Temperature Range		-40	-	+85	°C

DW9255 used as 2nd IF filter for GP2010

Centre Frequency	35.42MHz
Pass Band	±1.0MHz (within ±1.0dB)
Insertion loss	14-18dB
3rd IF Image frequency at 2nd IF	26.8MHz
Source Impedance	500Ω typical
Load Impedance	1000Ω typical

The second external IF filter is connected between the output of Stage 2 and input of Stage 3. It is required to define the bandwidth of the RF section of the GPS receiver, hence it is critical to the receiver performance. The filter should be flat across the 2MHz bandwidth of the GPS Coarse-Acquisition (C/A) code signal. It should also have high rejection (greater than 20dB) beyond this bandwidth, and so should have a brick-wall type response at these extremes. The DW9255 SAW filter provides a 1dB Bandwidth of typically 1.9MHz centred on 35.42MHz, with a typical pass band ripple of 0.8dB, when the SAW input and output capacitance is resonantly matched with inductors of optimum value. The out-of-band signal rejection is better than 21dB at ±2.0MHz, and better than 35dB at ±7.5MHz.

The frequency response of the DW9255 SAW filter with matching components is shown in Fig. 3. The matching components used with the GP2010 device are shown in Fig. 4.

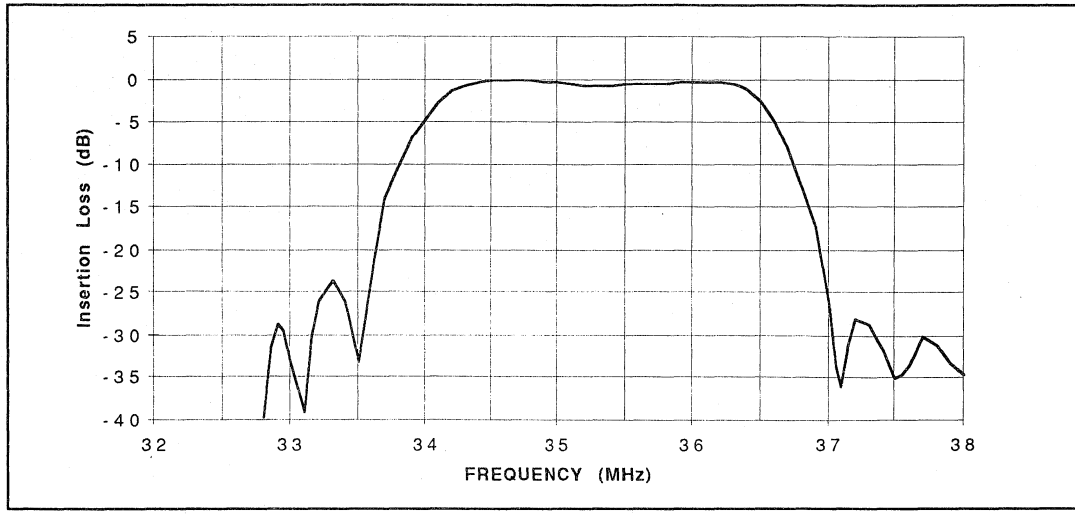


Fig.3 Typical frequency response of DW9255 SAW filter used as 2nd IF filter

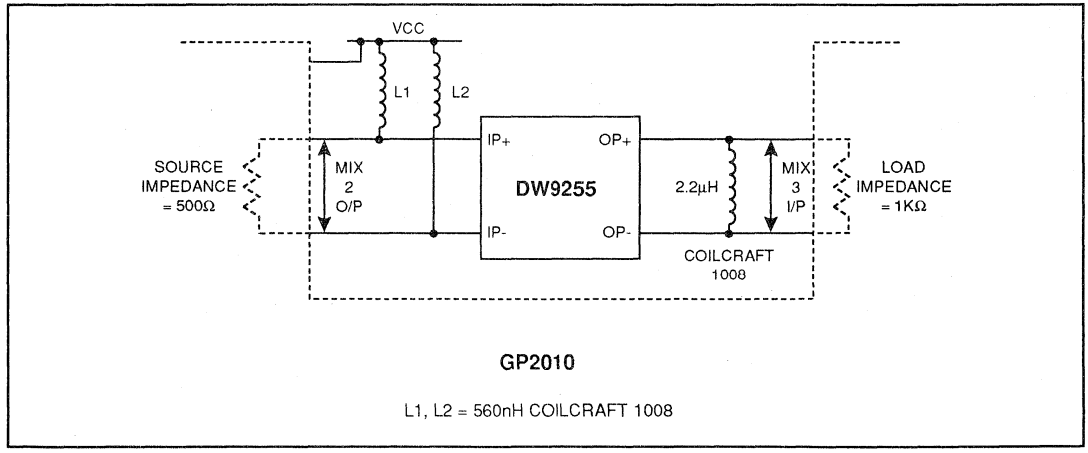


Fig.4 Typical matching components when used with GP2010 GPS Front-end IC

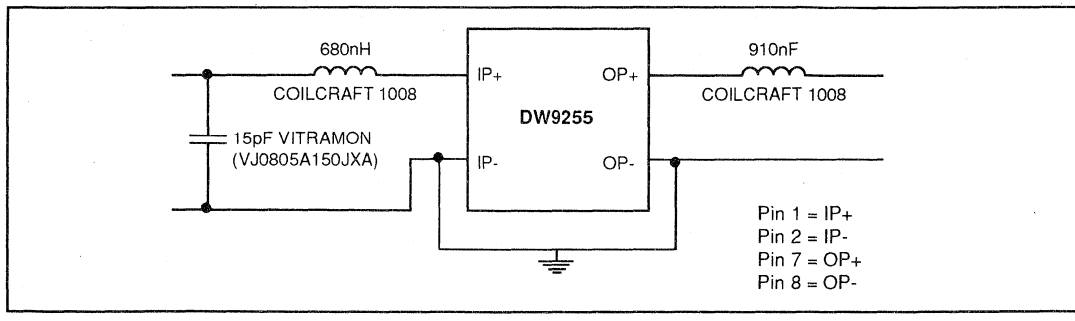


Fig.5 50Ω Matching network

Section 3
Digital Products

GEC PLESSEY
SEMICONDUCTORS

GP2021

GPS 12 CHANNEL CORRELATOR WITH MICROPROCESSOR SUPPORT FUNCTIONS

The GP2021 is a 12 channel C/A code baseband correlator for use in NAVSTAR GPS and GLONASS satellite navigation receivers. The GP2021 complements the GP2015 and GP2010 C/A code RF downconverters available from GEC Plessey Semiconductors.

The GP2021 is compatible with most 16 bit and 32 bit microprocessors, especially those from Motorola and Intel, with additional on–chip support for the ARM60 32 bit RISC processor. When the ARM60 is used, the on–chip memory management functions allow implementation of a full GPS receiver with minimal external logic.

The GP2021 allows individual channel de–activation, for systems not requiring full 12 channel operation, to save power and processor loading. Receiver power may be further conserved by reducing the supply voltage to 2.2V under battery backup. Although all system functions are disabled, the 32.768kHz oscillator and Real Time Clock are maintained for the microprocessor to estimate satellite visibility at power on to reduce signal acquisition time.

A development system called the GPS Builder–2 is available as a basis for receiver design using the GP2021 and associated products.

FEATURES

- 12 Fully Independent Correlation Channels
- 1PPS UTC Aligned Timing Output
- On–Chip Dual UART and Real Time Clock
- Compatible with most 16 and 32 bit Microprocessors
- Memory Control Logic for ARM60 Microprocessor
- Low Voltage, Low Current Power–Down Mode
- Power Dissipation 150mW Typical
- Compatible with GP2015 and GP2010 RF Front Ends
- Battery Backup Voltage 2.2V (min)

APPLICATIONS

- GPS Navigation Systems
- High Integrity Combined GPS–GLONASS Receivers
- GPS Geodetic Receivers
- Time Transfer Receivers

ORDERING INFORMATION

GP2021/IG/GQ1R

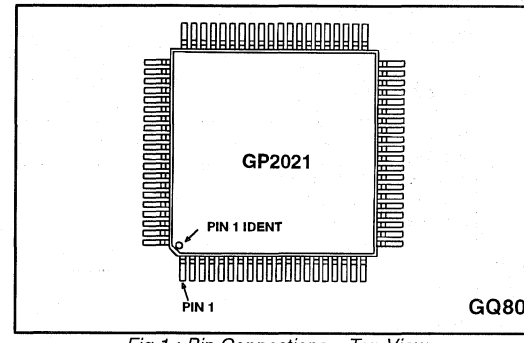


Fig.1 : Pin Connections – Top View

PIN	DESCRIPTION	PIN	DESCRIPTION
1	MULTI_FN_IO	41	A6
2	POWER_GOOD	42	A5
3	NRESET_OP	43	A4
4	NARMSYS	44	A3
5	XIN	45	A2
6	XOUT	46	A1 / ALE_IP
7	TXA	47	A0 / NRESET_IP
8	TXB	48	D0
9	RXA	49	D1
10	RXB	50	D2
11	NROM / NC	51	D3
12	NEEPROM / NC	52	D4
13	NSPARE_CS / NC	53	D5
14	V_{DD}	54	D6
15	V_{SS}	55	V_{DD}
16	NRAM / NC	56	V_{SS}
17	NW0 / NC	57	D7
18	NW1 / NC	58	D8
19	NW2 / NC	59	D9
20	NW3 / NC	60	D10
21	NRD / NC	61	D11
22	ARM_ALE / NC	62	D12
23	DBE / NC	63	D13
24	ACCUM_INT	64	D14
25	MEAS_INT	65	D15
26	NBW / WRPROG	66	PLL_LOCK
27	NMREQ / DISCIP2	67	V_{DD}
28	NOPC / NINTELMOT	68	DISCOP
29	NRW / DISCIP3	69	V_{SS}
30	MCLK / NC	70	CLK_T
31	ABORT / MICRO_CLK	71	CLK_I
32	DISCIO	72	V_{SS}
33	A22 / READ	73	SAMPCLK
34	V_{DD}	74	V_{DD}
35	V_{SS}	75	NBRAM / DISCIP4
36	A21 / NCS	76	SIGN0
37	A20 / WREN	77	MAG0
38	A9	78	SIGN1
39	A8	79	MAG1
40	A7	80	DISCIP1

TABLE OF CONTENTS

RELATED PRODUCTS

PART	DESCRIPTION	DATASHEET REFERENCE
GP2015	Global Positioning System Receiver RF Front End – TQFP 48 package	DS4374
GP2010	Global Positioning System Receiver RF Front End – PQFP 44 package	DS4056
DW9255	35.42MHz SAW Filter	DS3861
P60ARM	32 bit RISC Microprocessor	DS3553
GPS Builder–2	Global Positioning System 12 Channel Receiver Development System	DS4004

TYPICAL GPS RECEIVER

Fig. 2 shows a typical GPS receiver employing a GP2010 RF front–end, a GP2021 correlator and an ARM60 32 bit RISC microprocessor.

A single front end may be used, since all GPS satellites use the same L1 frequency of 1575.42 MHz. However, in order to achieve better sky coverage, it is sometimes desirable to use more than one antenna. In this case, separate front ends will be needed.

The RF section, GP2010, performs down conversion of the L1 signal for digital baseband processing. The resultant signal is then correlated in the GP2021 with an internally generated replica of the satellite code to be received. Individual codes for each channel may be selected independently to enable acquisition and tracking of up to 12 different satellites simultaneously.

The results of the correlations form the accumulated data and are transferred to the microprocessor to give the broadcast satellite data (the 'Navigation Message') and to control the software signal tracking loops.

The GP2021 can be interfaced to one of two styles of front end. In Real_Input mode, the front end supplies either a 1 (sign) or 2 (sign and magnitude) bit signal to either the SIGN0/MAG0 or SIGN1/MAG1 inputs of the GP2021. Alteratively, in Real_Input mode, 2 separate front ends can be connected to a single GP2021 and selected under software control. The GP2015 and GP2010 are Real_Input mode front ends.

In Complex_Input mode, the front end is required to supply In–phase (I) and Quadrature (Q) signals to the SIGN0/MAG0 and SIGN1/MAG1 inputs respectively. Hence, only a single front end can be used with each GP2021 in Complex_Input mode.

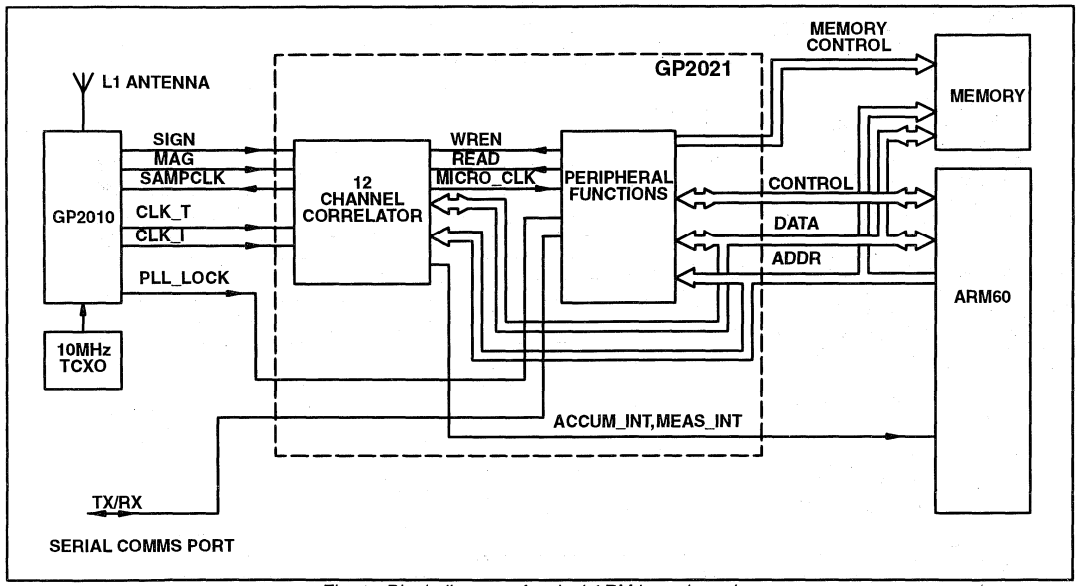


Fig. 2 : Block diagram of typical ARM based receiver

PIN DESCRIPTION

All V_{SS} and V_{DD} pins must be connected in order to ensure reliable operation. Any unused inputs must be tied High or Low. The Table below describes the pin functions in Real_Input mode and assumes a master clock input frequency of 40MHz. Those pins whose functions differ in Complex_Input mode are described at the end of the table.

Note that those pin names containing a '/' have dual functionality between ARM System and Standard Interface modes. The Pin mnemonic for ARM System mode always precedes the '/'.

Pin No	Signal Name	Type	Description ARM System Mode	Description Standard Interface Mode
15, 35, 56, 69, 72	V_{SS}	–	Ground Pin.	
14, 34, 55, 67, 74	V_{DD}	+	Power supply to device.	
1	MULTI_FN_IO	I/O	Multi–function input / output. Its function is configured by the IO_CONFIG register. After a GP2021 reset it acts as the Digital System Test Enable input. It can also be configured as a discrete output, or a discrete input if certain conditions are met.	Can be configured as the TRIGGER input to the DEBUG block in ARM System mode.

Pin No	Signal Name	Type	Description ARM System Mode	Description Standard Interface Mode
2	POWER_GOOD	I	Power Monitor input. High for normal operation. Low forces the GP2021 into Power Down mode.	
3	NRESET_OP	O	System Reset output (Active Low). Lasts for 4 MICRO_CLK cycles after all reset conditions have cleared.	
4	NARMSYS	I	Processor Mode Selection input. When Low, this input selects ARM System mode. When High, Standard Interface mode is selected.	
5	XIN	I	Crystal input connection to Real Time Clock.	
6	XOUT	O	Crystal output connection from Real Time Clock.	
7	TXA	O	Transmit Data output from Channel A of the Dual UART.	
8	TXB	O	Transmit Data output from Channel B of the Dual UART.	
9	RXA	I	Receive Data input to Channel A of the Dual UART. This pin acts as a master clock input in Digital System Test mode.	
10	RXB	I	Receive Data input to Channel B of the Dual UART. This pin acts as the Real Time Clock reset in Digital System Test mode.	
11	NROM / NC	O	ROM Chip Select output (Active Low).	Unused output. (Do not connect.)
12	NEEPROM / NC	O	EEPROM Chip Select output (Active Low).	Unused output. (Do not connect.)
13	NSPARE_CS / NC	O	Spare Chip Select output (Active Low).	Unused output. (Do not connect.)
16	NRAM / NC	O	RAM Chip Select output (Active Low).	Unused output. (Do not connect.)
17	NW0 / NC	O	Byte 0 Write Strobe output (Active Low).	Unused output. (Do not connect.)
18	NW1 / NC	O	Byte 1 Write Strobe output (Active Low).	Unused output. (Do not connect.)
19	NW2 / NC	O	Byte 2 Write Strobe output (Active Low).	Unused output. (Do not connect.)
20	NW3 / NC	O	Byte 3 Write Strobe output (Active Low).	Unused output. (Do not connect.)
21	NRD / NC	O	Read Data Strobe output (Active Low).	Unused output. (Do not connect.)
22	ARM_ALE / NC	O	ALE output to the microprocessor (Active High). Controls the transparent latches at the microprocessor address outputs.	Unused output. (Do not connect.)
23	DBE / NC	O	Data Bus Enable output to the microprocessor. When Low, places the microprocessor data bus drivers in a high impedance state.	Unused output. (Do not connect.)
24	ACCUM_INT	O	A free running interrupt to the microprocessor. It allows control of data transfer between the accumulators in the correlator and the microprocessor. It is active Low when configured for ARM System mode or Motorola mode and is active High in Intel mode.	
25	MEAS_INT	O	An interrupt to the microprocessor. It allows control of measurement data transfer between the correlator and the microprocessor. It is active Low when configured for ARM System mode or Motorola mode and is active High in Intel mode.	
26	NBW / WRPROG	I	Byte/Word input from the microprocessor. Low indicates a byte transfer, and High a word transfer.	Write–Read Program input. In Intel mode, High selects 486 style interface and Low 186 style. Unused in Motorola mode.
27	NMREQ / DISCIP2	I	Memory Request input from the microprocessor. Low indicates that the microprocessor requires a memory access during the following cycle.	Multi–purpose discrete input.
28	NOPC / NINTELMOT	I	Opcode fetch input from the microprocessor. Low indicates that an instruction is being fetched and High that data is being transferred.	High selects Motorola mode and Low Intel mode.
29	NRW / DISCIP3	I	Read/Write Select input from the microprocessor. Low indicates a read cycle and High a write cycle.	Multi–purpose discrete input.
30	MCLK / NC	O	Microprocessor Clock output (nominally 20MHz). Its phases can be stretched under control of the Microprocessor Interface.	Unused output. (Do not connect.)

Pin No	Signal Name	Type	Description ARM System Mode	Description Standard Interface Mode
31	ABORT / MICRO_CLK	O	Abort output to the microprocessor. Generates a valid ARM Data Abort sequence, triggered by a rising edge at MULTI_FN_IO if this function is enabled.	20MHz Clock output. Provides a 20MHz clock with a 1:1 mark–to–space ratio.
32	DISCIO	I/O	Multi–purpose discrete input / output. After a GP2021 reset it is configured as an input.	
33	A22 / READ	I	Address input from the microprocessor. A<22:20> are decoded to select the address space partitioning.	Read input from the microprocessor. In Intel mode it is the active Low read strobe. In Motorola mode it is the Read (High) / Write (Low) select line.
36	A21 / NCS	I	Address input from the microprocessor. A<22:20> are decoded to select the address space partitioning.	GP2021 Chip Select input (Active Low).
37	A20 / WREN	I	Address input from the microprocessor. A<22:20> are decoded to select the address space partitioning.	Write–Read Strobe input from the microprocessor. In Intel mode it is the active Low write strobe. In Motorola mode it is the active High Write–Read strobe.
38 – 45	A<9:2>	I	Address Inputs <9:2> from the microprocessor. These allow register selection.	
46	A1 / ALE_IP	I	Address input 1 from the microprocessor. A<1:0> are decoded to provide individual byte write selection via NW<3:0>.	Address Latch Enable input from microprocessor (Active High).
47	A0 / NRESET_IP	I	Address input 0 from the microprocessor. A<1:0> are decoded to provide individual byte write selection via NW<3:0>.	Reset input (Active Low).
48– 54, 57–65	D<0:15>	I/O	Bidirectional data bus.	
66	PLL_LOCK	I	PLL Lock Indicator input from RF section. When High this signal indicates that the PLL within the RF section is in lock and the master clock inputs have stabilised.	
68	DISCOP	O	Multi–purpose discrete output.	
70	CLK_T	I	Master clock input (40MHz).	
71	CLK_I	I	Inverted Master clock input.	
73	SAMPCLK	O	Sample Clock output to the front end. Provides a 5.714MHz clock with a 4:3 mark–to–space ratio.	
75	NBRAM / DISCIP4	I	Battery Backed RAM select input. Defines the state of the NRAM output in Power Down mode.	Multi–purpose discrete input.
76	SIGN0	I	SIGN0 input from the RF section.	
77	MAG0	I	MAG0 input from the RF section.	
78	SIGN1	I	SIGN1 input from a second, optional, RF section.	
79	MAG1	I	MAG1 input from a second, optional, RF section.	
80	DISCIP1	I	Multi–purpose discrete input.	

Differences between Real and Complex_Input Mode

The input mode is selected by the FRONT_END_MODE bit in the SYSTEM_SETUP register. It defaults to Real_Input mode at power up. The differences between Real and Complex input mode are summarised in the following table.

Description	Real_Input mode	Complex_Input mode
Recommended Master clock frequency	40MHz	35MHz
GP2021 internal clocking [1]	÷7	÷6
MICRO_CLK [2] output frequency mark : space	20MHz 1:1	17.5MHz 1:1
Pin No 76	SIGN 0	SIGN_I
Pin No 77	MAG 0	MAG_I
Pin No 78	SIGN 1	SIGN_Q
Pin No 79	MAG 1	MAG_Q
Input Signal Sampling Rate	5.714MHz	5.833MHz
SAMPCLK output frequency mark : space	5.714MHz 4:3	Not Available (held Low)

Notes. 1 The GP2021 interrupt and TIC timebase dividers are clocked by this resulting clock.
2 The MCLK output is derived from this signal. In ARM mode the phases of MCLK are stretched by the Microprocessor Interface block.

FUNCTIONAL DESCRIPTION

The GP2021 incorporates a 12 Channel GPS Correlator, together with microprocessor support functions including a Dual UART, a Real Time Clock and Memory Control Logic for the ARM60 microprocessor. It can be configured for either ARM System mode or Standard Interface mode. A block diagram of the GP2021 is shown in Fig. 3.

Whilst in ARM System mode the Memory Control Logic allows an ARM60 microprocessor to interface with the Correlator, Real Time Clock, Dual UART and a variety of memory devices (i.e. SRAM, EPROM, Flash and EEPROM), without the need for external glue logic.

In Standard Interface mode the GP2021 allows most 16 and 32 bit microprocessors to interface with the Correlator, Real Time Clock and Dual UART. More specifically, this mode allows the interface to be configured for either Intel or Motorola style microprocessor interfaces.

In the functional description which follows the correlator is described first, followed by the peripheral functions.

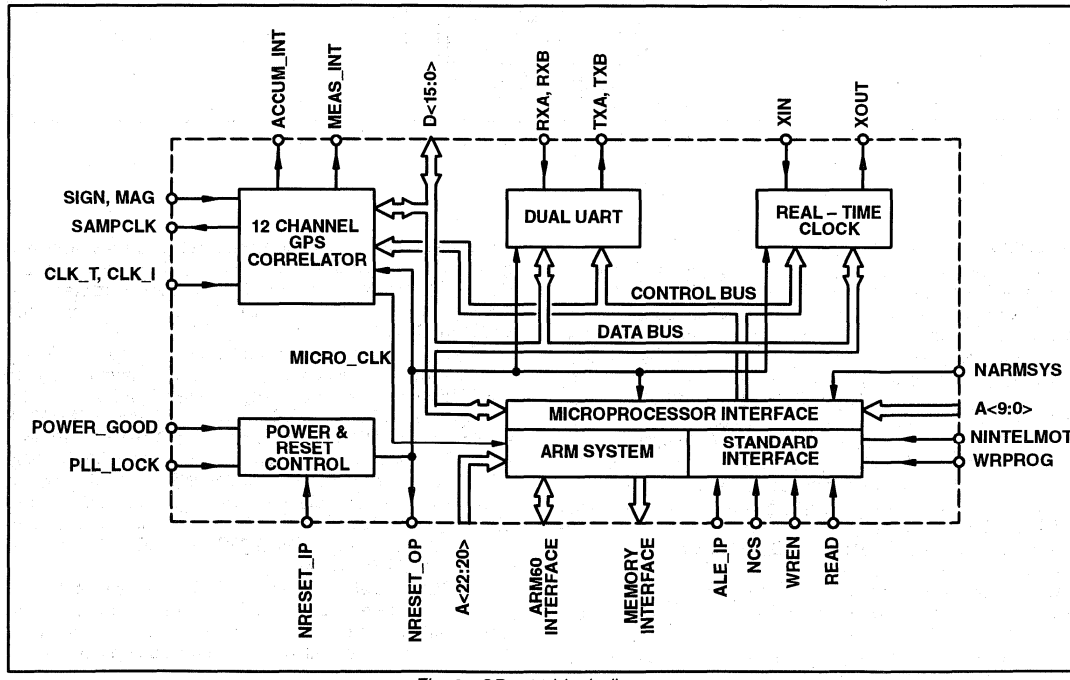


Fig. 3 : GP2021 block diagram

12 CHANNEL CORRELATOR

Fig. 4 shows a block diagram of the correlator. It consists of the following blocks:

Clock Generator

The Clock Generator block divides the frequency of the master clock CLK_T/CLK_I by 6 or 7 to give the internal multi–phase set of clocks. When in Real_Input mode CLK_T/CLK_I will normally be a 40MHz clock, which is divided by 7. When in Complex_Input mode it will normally be at 35MHz which is divided by 6. The SAMPCLK pin is an output giving a 4:3 mark–to–space ratio clock at 40 MHz / 7 (= 5·714 MHz) in Real_Input Mode.

The Clock Generator also produces the MICRO_CLK signal at half the master clock frequency (20 MHz for Real _Input mode, 17.5 MHz for Complex_Input mode) with a 1:1 mark–to–space ratio. This signal is output on the MICRO_CLK pin in Standard Interface mode. However, its main purpose is that of a synchronising clock to the memory control logic in ARM System Mode and it is from this that the processor clock output, MCLK, is derived.

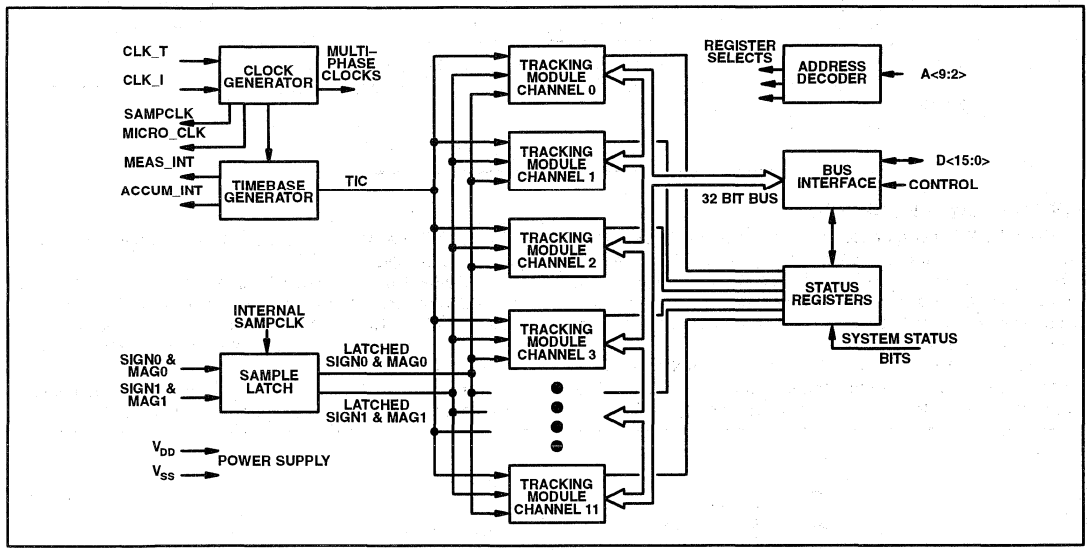


Fig. 4 : Correlator block diagram

Timebase Generator

The Timebase Generator produces 4 important timing signals: ACCUM_INT, TIC, MEAS_INT and TIMEMARK.

ACCUM_INT is an interrupt provided to control data transfer between the correlator accumulators and the microprocessor. It may be detected by means of the ACCUM_INT output or by reading the ACCUM_STATUS_A register (where bit 15 is a flag indicating that ACCUM_INT has occurred since the previous read of this register). ACCUM_INT is cleared by reading ACCUM_STATUS_A.

After power–up this interrupt occurs every 505.05µs. Its period can subsequently be changed in one of 3 ways:

1) toggling the FRONT_END_MODE bit of the SYSTEM_SETUP register,
2) toggling the INTERRUPT_PERIOD bit of the SYSTEM_SETUP register, or
3) writing directly to the PROG_ACCUM_INT register.

See section "Detailed Description of Registers" on page 25 for more information.

TIC is an internal signal with a default period of 99999.90µs. It is used to latch measurement data (Epoch count, Code phase, Code DCO phase, Carrier DCO phase and Carrier cycle count) of all 12 channels at the same instant. Its period can subsequently be changed, by writing to the PROG_TIC_HIGH and PROG_TIC_LOW registers, or toggling the FRONT_END_MODE bit of the SYSTEM_SETUP register.

MEAS_INT is a signal derived from the TIC counter. It may be used by the microprocessor as a software module switching interrupt either by using the MEAS_INT output or by reading the ACCUM_STATUS_B or MEAS_STATUS_A register. MEAS_INT is activated at each TIC and 50 ms before each TIC so long as the TIC period is greater than 50 ms. If the TIC period is less than 50 ms, MEAS_INT is activated only at each TIC. It is cleared by reading either the ACCUM_STATUS_B or MEAS_STATUS_A register, depending upon the MEAS_INT_SOURCE bit of the SYSTEM_SETUP register.

TIMEMARK is also derived from TIC and may be output on one of the discrete output pins. This signal is intended to be used as an accurate 1 Pulse Per Second timing reference, aligned to UTC (Universal Time Co–ordinated system), with a pulse width of 1ms.

TIMEMARK has two methods of operation but in both

cases TIMEMARK rising edges are generated co–incident with the rising edges of TIC. Therefore, for TIMEMARK to be aligned with UTC, TIC must be aligned with UTC. This is done by modifying the TIC period for a single TIC cycle, then setting it back to its original value, thus slewing the phase of TIC. TIMEMARK may be generated by setting the TIMEMARK_ARM bit in the TIMEMARK_CONTROL register, in which case the next TIC will generate a rising edge at TIMEMARK and clear the TIMEMARK_ARM bit. Alternatively TIMEMARK may be generated as a programmable integer number of TIC's, again under the control of the TIMEMARK_CONTROL register.

Status Registers

There are four status registers (ACCUM_STATUS_A, _B, _C and MEAS_STATUS_A). These contain flags associated with the accumulated and measurement data held on each of the 12 channels. Some system level status bits also appear in these registers.

Sample Latches

The Sample Latches synchronise data from the front end to the internal SAMPCLK.

In Real_Input mode the down converted satellite signal can be sampled at the output of the front end by SAMPCLK. This data is then input to the GP2021 as 2 bit data on either the SIGN0, MAG0, or SIGN1, MAG1 inputs, where it is re–sampled at the next rising edge of SAMPCLK. These signals are then distributed to the 12 tracking modules.

When a GP2015 or GP2010 front end is used, the data represents a band–limited signal at an IF centered on 4.309MHz. Sampling at 5.714MHz aliases it to an IF of 1.405MHz.

In Complex_Input mode, the down converted satellite signal is applied direct to the GP2021 at its SIGN0, MAG0, SIGN1, MAG1 inputs, which act as In–Phase Sign, In–Phase Magnitude, Quadrature Sign and Quadrature Magnitude respectively. These signals are sampled at 5.833MHz within the correlator and then passed to the tracking modules.

Address Decoder

The Address Decoder performs address decoding for the correlator.

Bus Interface

The Bus Interface controls the transfer of data between the external 16 bit wide data bus and the internal 32 bit data bus.

Apart from the code and carrier DCO increment values, all data transfers are 16 bits wide. Write operations to the code and carrier DCO's are 32 bit data transfers, in which the High 16 bit word must be written immediately before the low 16 bit word. Note that the write cycle to write cycle delay of 300 ns referred to in the Microprocessor Interface does not apply between the first and second write cycles for 32 bit DCO data transfers. For further information see the Microprocessor Interface section.

TRACKING MODULES

The Tracking Modules are 12 identical signal tracking channels numbered CH0 to CH11, each with the block diagram shown in Fig 5. These blocks generate the data used to track the satellite signals. There is no overwrite protection mechanism on this data. For further information see the section on CONTROLLING THE GP2021.

Each Tracking Channel can be individually programmed to operate in either Update or Preset mode. Update mode is the normal mode of operation. Preset mode is a special mode of operation where writes to certain registers are delayed until the next TIC to allow synchronisation of registers and presetting of the code DCO phase. For further information see the Preset Mode section in the Detailed Operation of the GP2021.

The individual sub–blocks in the tracking modules are:

Carrier DCO

The Carrier DCO, which is clocked at the SAMPCLK frequency, is used to synthesise the digital local oscillator signal required to bring the input signal to baseband in the mixer block, and must be adjusted away from its nominal value to allow for Doppler shift and reference frequency error.

When used with the GP2015/GP2010 the nominal frequency of this signal is 1·405396825 MHz (with a resolution of 42.57475 mHz) and is set by loading the 26 bit register CHx_CARRIER_DCO_INCR. This very fine resolution is needed so that the DCO will stay in phase with the satellite signal for an adequate time. The Carrier DCO Phase cannot be directly set, but must be adjusted by altering the frequency.

The Carrier DCO outputs are 4 level, 8 phase sinusoidals with the following sequences over one cycle:

Destination Arm	Sequence
I_{LO}	–1+1+2+2+1–1–2–2
Q_{LO}	+2+2+1–1–2–2–1+1

Table 1 Carrier DCO outputs

As the clock to the DCO is normally less than 8 times the output frequency, not all phases are generated in every cycle. With a typical clock frequency of 5·714 MHz and an output frequency of 1·405 MHz there are only around 4 phases per cycle. These will slide through the cycle as time progresses to cover all values.

Code DCO

The Code DCO is similar to the Carrier DCO block. It is also clocked at the SAMPCLK frequency and synthesises the oscillator required to drive the code generator at twice the required chipping rate. The nominal frequency of the output is 2·046 MHz, to give a chip rate of 1·023 MHz and is set by loading the 25 bit register CHx_CODE_DCO_INCR.

It is programmed with a resolution of 85·14949 mHz when used with a GP2015/GP2010 front end. The very fine resolution is again needed to keep the DCO in phase with the satellite signal. The Code DCO Phase can only be set to the exact satellite phase in Preset mode. In Update mode, it must be aligned with the satellite phase by adjusting its frequency.

Carrier Cycle Counter

The Carrier Cycle Counter is 20 bits long, and keeps a count of the number of cycles of the Carrier DCO between TIC's. This is not needed for a basic navigation system but may be used to measure the range change (delta–range) to each satellite between TIC's. The delta ranges can be used to smooth the code pseudo–ranges. For finer detail the Carrier DCO phase may also be read at each TIC to give the fractional part of the cycle count or delta–range.

C/A Code Generator

The C/A Code Generator generates the selected Gold code for a GPS satellite (1 to 32), a ground transmitter (pseudolite, 33 to 37), an INMARSAT–GIC satellite (201 to 211) or a GLONASS satellite. A Gold code is selected by writing a specific pattern of 10 bits, as listed in the section 'Detailed Description of Registers', to the CHx_SATCNTL register, or by setting the GPS_NGLON bit to Low for the GLONASS code. Two outputs are generated to give both a PROMPT and a TRACKING signal. The TRACKING signal can be set to one of four modes: EARLY (one half chip before the PROMPT signal), LATE (one half chip behind), DITHERED (toggled between EARLY and LATE every 20ms) or EARLY–MINUS–LATE (the signed difference).

The output code is a sequence of +1's and –1's for all code types except EARLY–MINUS–LATE where the result can also

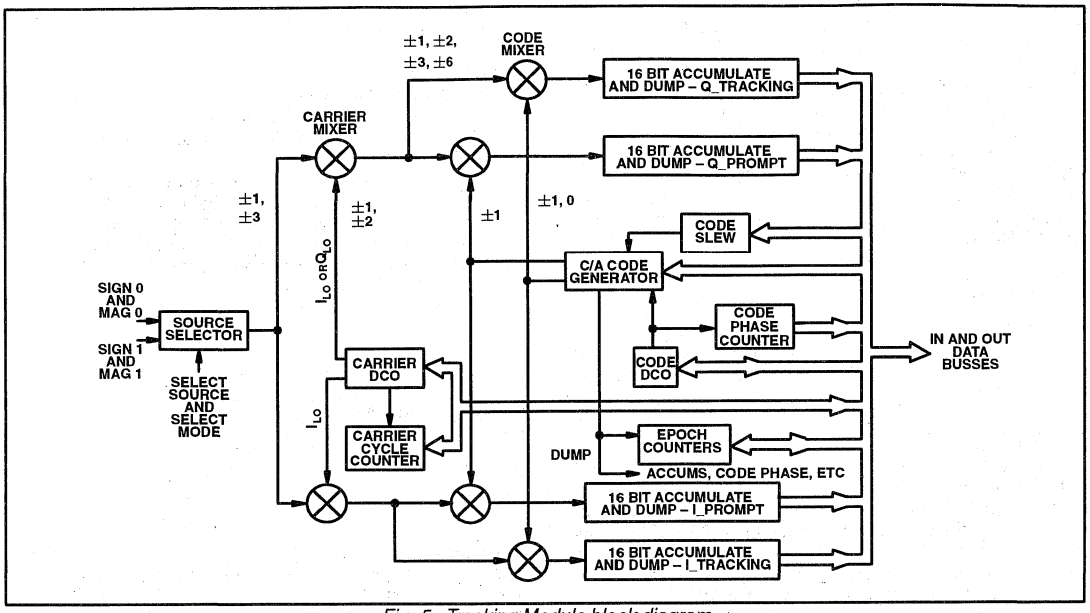


Fig. 5 : Tracking Module block diagram

be a 0. To avoid having an unused LSB in the accumulators, the values in EARLY–MINUS–LATE mode are halved from the +2, 0, –2 that results from the calculation (+1 or –1) – (+1 or –1) to +1, 0, –1. This must be considered when choosing thresholds in the software, as the correlation results will be exactly half of the values otherwise expected.

At the end of every code sequence (1023 chips in GPS mode or 511 chips in GLONASS mode) a DUMP signal is generated to latch the Accumulated Data for use by the signal tracking software. Each channel is latched separately, as the satellite signals are not received in phase with each other.

Source Selector

In Real_Input mode the Source Selector selects which input signal pair to use (SIGN0/MAG0 or SIGN1/MAG1). In Complex_Input mode SIGN0/MAG0 are passed to the In–phase arm and SIGN1/MAG1 to the Quadrature arm. The data is treated as having the values shown in Table 2 below (in both modes):

Sign	Mag	Value
0	1	–3
0	0	–1
1	0	+1
1	1	+3

Table 2: SIGN/MAG values

Carrier Mixers

The Carrier Mixers multiply the digital input signal by the Carrier DCO digital local oscillator to generate a signal at baseband. In Real_Input mode both I and Q Carrier DCO phases are directed to the appropriate mixers. In Complex_Input mode a single In–Phase Carrier DCO output is used in both mixers since the input signal is already in I and Q form. The mixing of the Carrier DCO outputs with the input signal produces a baseband signal which can have the values ±1, ±2, ±3 and ±6.

Code Mixers

The Code Mixers multiply the I and Q baseband signals from the Carrier Mixers with both the PROMPT and TRACKING local replica codes to produce 4 separate correlation results. The correlation results are passed to the Accumulate and Dump blocks for integration.

Accumulate and Dump

The Accumulate and Dump blocks integrate the Mixer outputs over a complete code period of nominally 1ms.

There are 4 separate 16 bit accumulators for each channel. These represent the correlation of the I and Q signals with the PROMPT and TRACKING codes, over the integration period. There is no overwrite protection mechanism on these registers so the data must be read before the next DUMP.

Code Phase Counter

The Code Phase Counter counts the number of half–chips of generated code and stores this value in the CHx_CODE_PHASE register on each TIC.

Code Slew Counter

The Code Slew Counter is used to slew the generated code by a number of half chips in the range 0 to 2047. In Update mode the slew occurs following the next DUMP. In preset mode it occurs at the next TIC. All slew operations are relative to the current code phase. The Code Slew counter must be written to each time a slew is required.

During the slewing process the accumulators for the channel being slewed are inhibited so that the first result is valid. If a slew is written while a channel is disabled it will occur as soon as the channel is enabled.

Epoch Counter

The Epoch Counters keep track of the number of code periods over a 1 second interval. This is represented by a 5 bit word for the number of 1 ms integration periods (0 to 19), plus a 6 bit word containing the number of 20 ms counts (0 to 49). The Epoch Counters can be pre–loaded to synchronise them to the data stream coming from the satellite. This value will be transferred immediately to the counter when in Update mode, or after the next TIC if in PRESET Mode.

The Epoch Counter values are latched on each TIC into the CHx_EPOCH register. In addition the instantaneous values are available from the CHx_EPOCH_CHECK register.

PERIPHERAL FUNCTIONS

The following section describes the Dual UART, Real Time Clock and Watchdog, Power and Reset Control and Discrete I/O blocks.

Dual UART

A Dual UART is included for serial communications. It has 2 identical blocks, UART_A and UART_B, each containing separate transmit and receive channels. The parity and separate transmit and receive baud rate can be configured independently for each UART. Each uses a polled processor interface and each transmit and receive channel has an 8 byte deep FIFO.

For further information on the UART registers refer to the Detailed Description of Registers and the GP2021 Register Map.

A typical serial data stream is shown in Fig. 6. The Parity bit is optional and if no parity is selected the time slot for it is removed from the data stream and the Stop bit follows immediately after the last data bit in both transmit and receive directions. Note that the LSB is always preceded by a Start bit. Table 3 shows possible UART configurations.

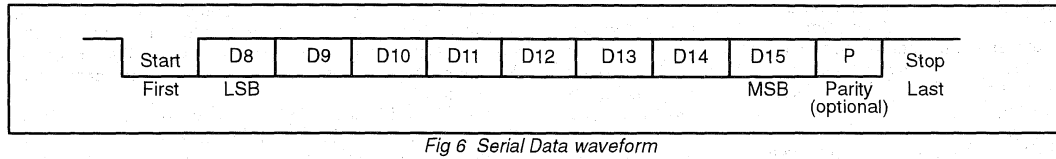


Fig 6 Serial Data waveform

Parameter	Value
Start bits	1 bit Low
Data bits	8 bits Logic 0 = Low Logic 1 = High
Stop bits	1 bit High
Parity	Odd/Even/None
Flow control	None
Transmit FIFO depth	8 bytes
Receive FIFO depth	8 bytes
FIFO speed	Transmit FIFO write rate and Receive FIFO read rate maximum is one byte per 230ns. The maximum buffer through delay is 2µs.
Data rate	300, 600,1.2k, 2.4k, 4.8k, 9.6k, 19.2k, 38.4k and 76.8k baud. Transmit and Receive rates individually configured.

Table 3 UART Functionality

Receiver

The incoming data streams on RXA, RXB are sampled by a clock at nominally 20 times the data rate, to search for an incoming Start bit. Once the receiver is synchronised to the data stream, each data bit is sampled only at its nominal centre to avoid errors due to slow or noisy bit edges. The receiver will resynchronise to each Start bit to prevent the accumulation of phase errors.

Only valid data (having correct Start, Stop and Parity bits) will be stored in the receiver FIFO. If a received word contains a parity or framing (Start/Stop bit) error, the appropriate flag bit will be set in the status register. If too many valid data words are received for the FIFO to hold, the excess will not be written into the FIFO, and an Overflow bit will be set in the status register. When receiving a continuous transmission, the Start bit of one word will follow immediately after the Stop bit of the preceding word. At lower word rates, a High is expected between words. The receiver will accept data with a baud rate error of up to ±1%.

Transmitter

Data is transmitted on pins TXA and TXB. In continuous transmission, the Start bit of one word will follow immediately after the Stop bit of the preceding word. At lower word rates, a High is sent between words.

If too many data words are written by the microprocessor to the UART for the transmitter FIFO to hold, the excess will not be stored. The UART will resume normal operation as soon as space becomes available. To avoid data loss, the software should limit the transmit data rate by either: keeping track of the number of bytes sent and the time to transmit them, or should read the Status register and stop writing when the Full bit is set.

Reset

It is possible for the software to reset either UART independently via the RESET_CHx registers. A hardware reset affects both UARTs. During a UART reset, the contents of all Control, and Status registers will be cleared. In addition

the Transmit and Receive FIFO's will be emptied and the TX outputs will be held Low.

Channel Loopback

For system test purposes, a loopback facility is provided for each channel, controlled by the Configuration registers. In loopback, the TX output is set High.

Real Time Clock (RTC) and Watchdog

This block consists of a 32.768kHz crystal oscillator, a fixed divider, a 24 bit counter, a Watchdog function and three 8 bit data registers. XIN and XOUT are the crystal in and crystal out connections to the oscillator circuit. A recommended crystal oscillator circuit is shown in Fig. 7. When the Real Time Clock is not being used, XIN must be tied Low.

The first divider is a fixed divide by 32768 giving a 1 Hz output. The counter then counts seconds, giving a maximum time of 194 days. The time is output in three 8 bit registers with the data being latched when a read is performed to the LS register (The register holding the least significant byte of the clock data). On reaching its maximum count, the count is frozen (i.e. all 1's), until being reset.

In Power Down mode the Real Time Clock continues to run, but access to the data registers is not allowed. When normal power is restored, the software can determine the elapsed time whilst in Power Down mode, thereby assisting in estimating the current position of GPS satellites and so reducing Time–To–First–Fix.

The Watchdog generates a System Reset (see Power And Reset Control) if the Watchdog Reset address has not been written to for a period of approximately 2s. The watchdog function is inhibited whilst in Power Down mode and can be disabled via a bit in the System Configuration register.The software is able to reset the Real Time Clock and Watchdog via the Clock Reset and Watchdog Reset registers respectively. In addition the watchdog is reset during a System Reset.

For further information on the registers refer to the section Detailed Description of Registers.

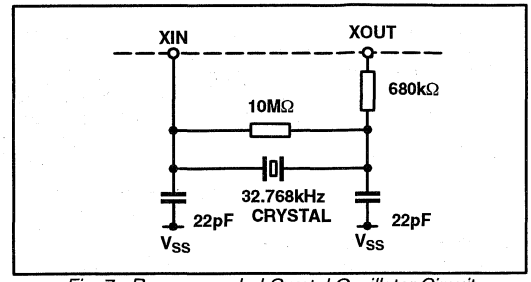


Fig. 7 : Recommended Crystal Oscillator Circuit

Power and Reset Control

This block performs 2 functions: Power Control and System Reset Generation

Power Down Mode

In order to allow power conservation within a battery backup system, the GP2021 provides a Power Down mode, in which the supply voltage may drop to a minimum of 2.2V, thereby minimising the supply current. In this mode all functions within the GP2021 are disabled except for the Real Time Clock.

The GP2021 is placed in Power Down mode by taking the POWER_GOOD pin Low. In ARM System mode with the NBRAM pin held Low, the initiation of Power Down mode is delayed until just after a falling edge of MICRO_CLK so as not to corrupt battery backed RAM. Fig. 8 shows a suggested circuit implementation. Table 4 shows output logic levels in Power Down mode.

In Power Down mode all inputs and I/Os except POWER_GOOD and XIN are internally switched to known logic levels to prevent extraneous switching from causing excessive power consumption, and may therefore be left floating. All the I/O pins (D<15:0>, MULTI_FN_IO and DISCIO) have their output drivers driven to the High Impedance state.

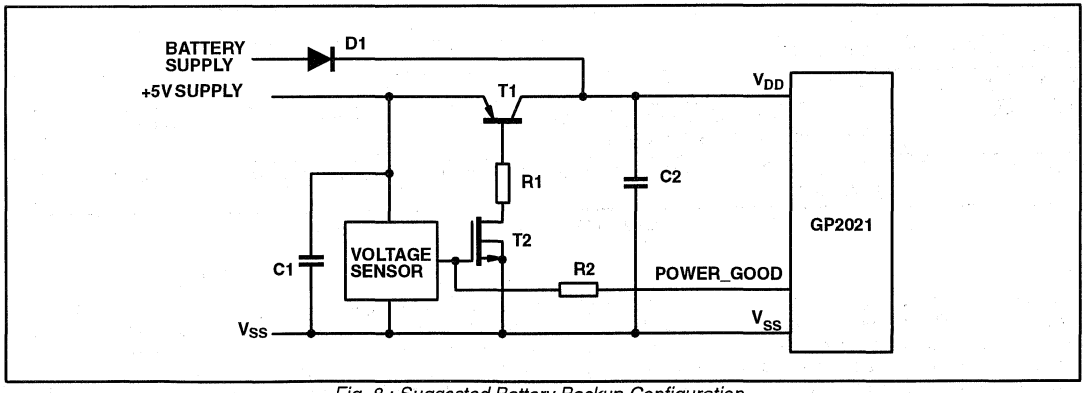


Fig. 8 : Suggested Battery Backup Configuration.

Pin Name	Logic Level
NW<3:0> / NC	Low
NRD / NC	Low
NRAM (standard interface mode)	Low
NRAM (ARM system mode)	$\overline{\text{NBRAM}}$
NROM / NC	High Impedance
NSPARE_CS/NC	High Impedance
NEEPROM / NC	High Impedance
TXA,TXB	Low
ACCUM_INT	High Impedance

Pin Name	Logic Level
MEAS_INT	High Impedance
ABORT / MICRO_CLK	Low
MCLK / NC	Low
ARM_ALE / NC	Low
DBE / NC	Low
NRESET_OP	Low
DISCOP	High Impedance
SAMPCLK	Low
XOUT	Active

Table 4 : Output Logic Levels in Power Down Mode

Hardware Reset Generation

The manner in which a hardware reset occurs depends on whether the GP2021 is in ARM System mode or Standard Interface mode. During a hardware reset, the NRESET_OP pin is taken Low and the reset signal is applied within the GP2021 to all blocks except the Real Time Clock.

There are 3 sources of hardware resets common to both ARM System and Standard Interface modes, with an additional source in Standard Interface mode:

POWER_GOOD: A hardware reset will occur if this pin is taken Low, as shown in Fig. 9. The purpose of this input is to detect a power failure. If the NBRAM pin is held Low in ARM System mode, the internal Power Down mode is not entered until about 6ns after the falling edge of MICRO_CLK, otherwise it is entered immediately. This allows for RAM write cycles to complete sensibly when Battery Backed–Up RAM is used, with no corruption of RAM data.

Watchdog: An expiry of the watchdog will result in a hardware reset as shown in Fig. 10. This reset will clear the watchdog whose time–out period is 2–3 seconds.

PLL_LOCK: The PLL_LOCK pin is used to indicate (when High),that the phase locked loop in the RF front end, which generates the master clock, is in lock. This signal is filtered within the GP2021 and the reset state associated with it is only de–activated if the PLL_LOCK input has been high for approximately 50 ms as shown in Fig. 11.

NRESET_IP: In addition to the 3 reset sources described above, an active Low NRESET_IP pin is available in Standard Interface mode if the system resets are to be generated externally. Fig. 12 shows a NRESET_IP generated reset.

Note that the NRESET_OP pin will go High 4 MICRO_CLK cycles after all hardware reset sources have cleared. This fulfills the reset requirements of the ARM60 microprocessor.

For information on the state of the registers following a hardware reset refer to the Detailed Description of Registers section.

System Error Status Register

This allows the software to determine whether the source of a hardware reset was from a power failure, a PLL_LOCK failure, watchdog timeout or from an external reset in Standard Interface mode. For further information refer to the Detailed Description of Registers section.

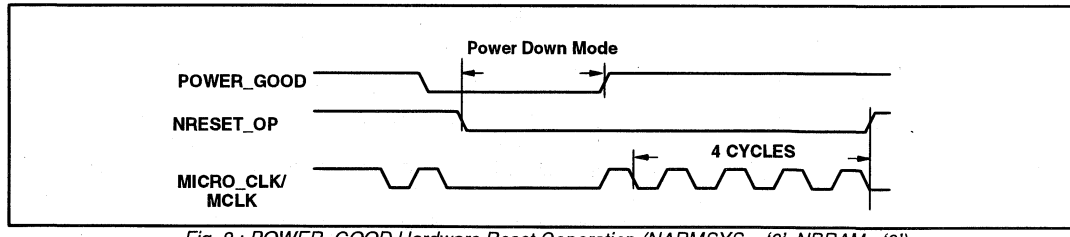


Fig. 9 : POWER_GOOD Hardware Reset Generation (NARMSYS = '0', NBRAM ='0')

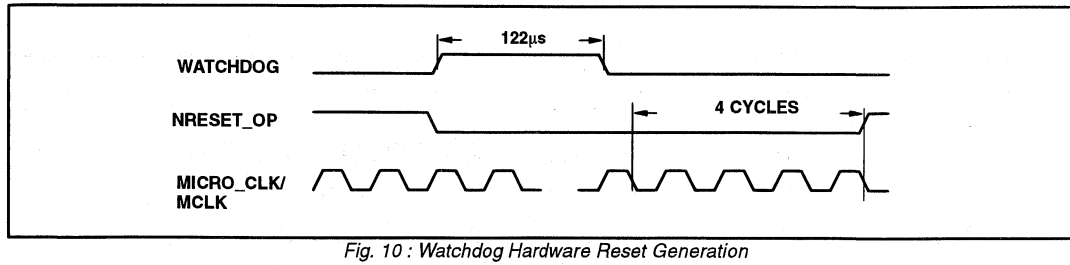


Fig. 10 : Watchdog Hardware Reset Generation

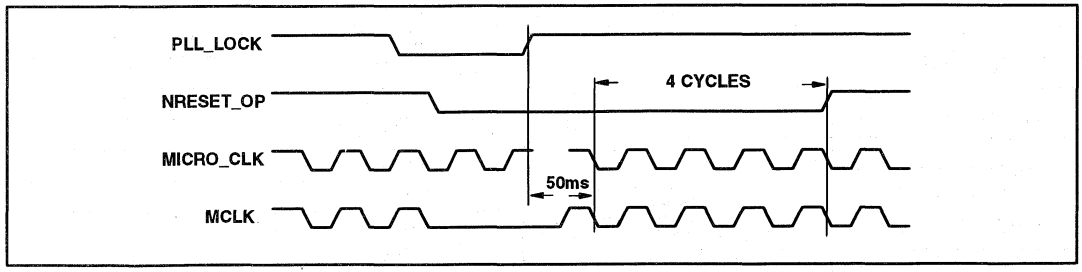


Fig. 11 : PLL_LOCK Hardware Reset Generation

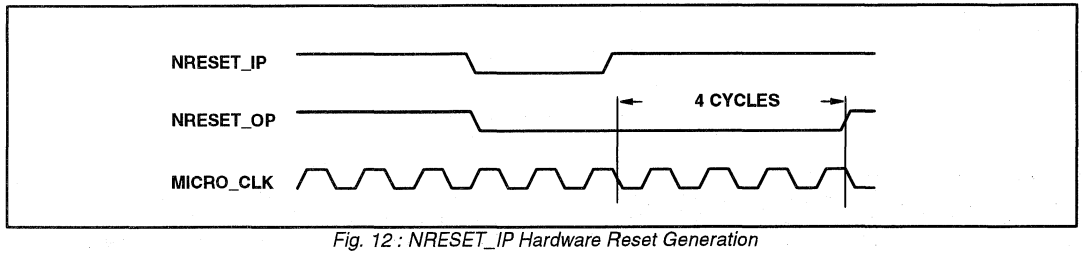


Fig. 12 : NRESET_IP Hardware Reset Generation

Discrete I/O

The GP2021 contains a number of pins which may be used as discrete inputs or discrete outputs for general purpose system monitoring and control applications. The actual pins which may be used for each function vary according to the application and the interface mode of the GP2021.Table 5 shows a list of possible discrete inputs and outputs and the modes in which they may be used. The level on all discrete inputs can be read from the IO_CONFIG register. The status of the DISCIP pin may also be read from ACCUM_STATUS_B. The discrete outputs are controlled via either the SYSTEM_SETUP or IO_CONFIG registers.

Discrete Inputs		
Pin Name	**Read Location**	**Conditions for use as Discrete Input**
NRW/DISCIP3	IO_CONFIG	Standard Interface mode.
NOPC/NINTELMOT	IO_CONFIG	ARM System mode (debug disabled).
NMREQ/DISCIP2	IO_CONFIG	Standard Interface mode.
NBW/WRPROG	IO_CONFIG	Motorola mode only.
DISCIO	IO_CONFIG	DISCIO configured as discrete Input.
NBRAM/DISCIP4	IO_CONFIG	Standard Interface Mode.
MULTI_FN_IO	IO_CONFIG	MULTI_FN_IO configured as discrete input.
SIGN0, MAG0	IO_CONFIG	Single real input mode (GP2010 or GP2015) front end using SIGN0, MAG0.
SIGN1, MAG1	IO_CONFIG	Single real input mode (GP2010 or GP2015) front end using SIGN1, MAG1.
DISCIP1	IO_CONFIG ACCUM_STATUS_B	Always available – dedicated Discrete Input.
RXA	IO_CONFIG	UART Channel A not used.
RXB	IO_CONFIG	UART Channel B not used.
Discrete Outputs		
Pin Name	**Configuration Location**	**Possible Outputs**
DISCOP	SYSTEM_SET_UP	High, Low, CH0 Dump, TIMEMARK, 100kHz Square Wave, Scan Out.
DISCIO	IO_CONFIG	High, Low, TIMEMARK, 100kHz Square Wave.
MULTI_FN_IO	IO_CONFIG	High, Low, TIMEMARK, 100kHz Square Wave.

Table 5 : Discrete Input/Output Configuration

Digital System Test Interface

The GP2021 contains a Digital System Test mode to allow testing of the digital section of the system board. Provided that the MULTI_FN_IO pin is High, this mode is enabled subsequent to a hardware reset or a write of specific data to the IO_CONFIG register. The enabling of Digital System Test mode has 3 effects:

(1) The master clock inputs, CLK_T and CLK_I, are replaced by the signal on the RXA pin. This allows the GP2021 to be clocked synchronously with the board tester which is relevant in ARM System mode where the GP2021 produces the main processor clock to the ARM60.

(2) The RXB pin becomes the active High RTC Reset input. This is mainly intended for factory testing of the GP2021, allowing the RTC to be reset on power up, but may also be used to disable the RTC and Watchdog circuits in this mode.

(3) The PLL_LOCK input and its associated 50ms delay as a reset source is overridden. This removes the dependency on the presence of the front end circuit.

MICROPROCESSOR INTERFACE

The Microprocessor Interface of the GP2021 is compatible with most 16 and 32 bit microprocessors. It can be configured for either ARM System mode or Standard Interface mode by means of the NARMSYS pin.

In Standard Interface mode, two mode control pins NINTELMOT and WRPROG are provided. NINTELMOT selects between Intel and Motorola style interfaces, with WRPROG selecting either Intel i486 or 80186 style interfaces. See Table 6 for more details.

NARMSYS	NINTELMOT	WRPROG	Mode	Processor
0	x	x	ARM System	ARM60
1	1	x	Standard Interface	Motorola style
1	0	0	Standard Interface	Intel 80186 style
1	0	1	Standard Interface	Intel 486 style

Table 6 Microprocessor Interface Configuration.

General Interface Timing

In addition to the detailed timings associated with individual read and write cycles (see Electrical Characteristics section), the internal architecture of the correlator also imposes limits on cycle to cycle timings (in particular write to write cycle and write to read cycle). For a simple microprocessor interface, it must be ensured that no attempts are made to access the correlator for the 300ns following the end of a correlator write cycle in Real_Input mode, or 314ns in Complex_Input mode. However, if the controlling software is to be allowed to write rapidly to the correlator (e.g. block writes), then a more complex bus interface (which inserts wait states) will be required. Note that this limitation only applies after correlator writes, not peripheral function writes, and also does not apply to writes to the correlator X_DCO_INCR_HIGH address.

The correlator section of the GP2021 uses a multi–phase clock internally, and the correlator registers load on specific clock phases. At the end of a write cycle, the falling edge of the internal write strobe latches both the relevant address and data bits. This data is then loaded from the internal data bus to the relevant register at some time during the following 300ns for Real_Input mode or 314ns for Complex_Input mode. A write cycle to the Correlator with no writes in the preceding 300ns (314ns) may be performed immediately, so long as the detailed signal timings are met. However, subsequent read or write cycles to the Correlator after this write cycle may need to be delayed if they would modify the internal address or data lines. Correlator read cycles with no write cycles in the preceding 300ns (314ns) are self–contained, and do not delay subsequent cycles. An isolated read cycle requires only sufficient wait states to meet the detailed signal timings.

Write Cycle To Read Cycle Timings

As described previously, the internal write cycle of the Correlator takes 300ns (314ns). Only once the write cycle is complete will the correlator address decoders switch to decoding the current address. The correlator uses a pre–charged internal data out bus and hence the decoded address lines must be stable before the internal bus drivers are enabled (when the read strobe goes high). Consequently, the read strobe must be held Low until some time after the end of the 300ns (314ns) internal write cycle, to allow sufficient internal address setup time. For the exact timing requirements see the Electrical Characteristics Section.

Write Cycle To Write Cycle Timings

The internal write cycle of the correlator takes 300ns (314ns) after the falling edge of the write strobe. During this time the write internal address and data busses (latched by write) must not be modified. If a second write follows the first, the second write cycle must be delayed such that it ends no earlier than 300ns (314ns) after the end of the previous write. The 'end' being a falling edge on the internal write strobe. The specific interface signal timings must also be met.

Notes about Interface Timing Constraints

It should also be noted that these timings need only be met for correlator accesses, not support function accesses, since these utilise self–contained write cycles and are not clocked by the multi–phase clocks. In addition, writes to the Correlator register X_DCO_INCR_HIGH need not incur subsequent delays since writes to this location do not instigate an internal write cycle. A write to this address must always be followed by a write to either a CHX_CARRIER_DCO_INCR_LOW or a CHX_CODE_DCO_INCR_LOW register and it is this second associated write which instigates the internal write cycle.

In ARM System mode all these timing requirements are handled by the internal memory manager.

Note that the exact number of wait states which need to be inserted after a correlator write is not fixed. If the processor were to perform a correlator write then spend 400ns accessing a different peripheral, subsequent correlator reads and writes would incur no additional delay. It is anticipated that correlator wait states will be generated by either one or two external counters, preset on the falling edge of a correlator write, and which then count down to zero. Only once the counter has reached zero may the next correlator access either complete (write) or start (read).

A series of correlator reads and writes are shown in Fig.13.

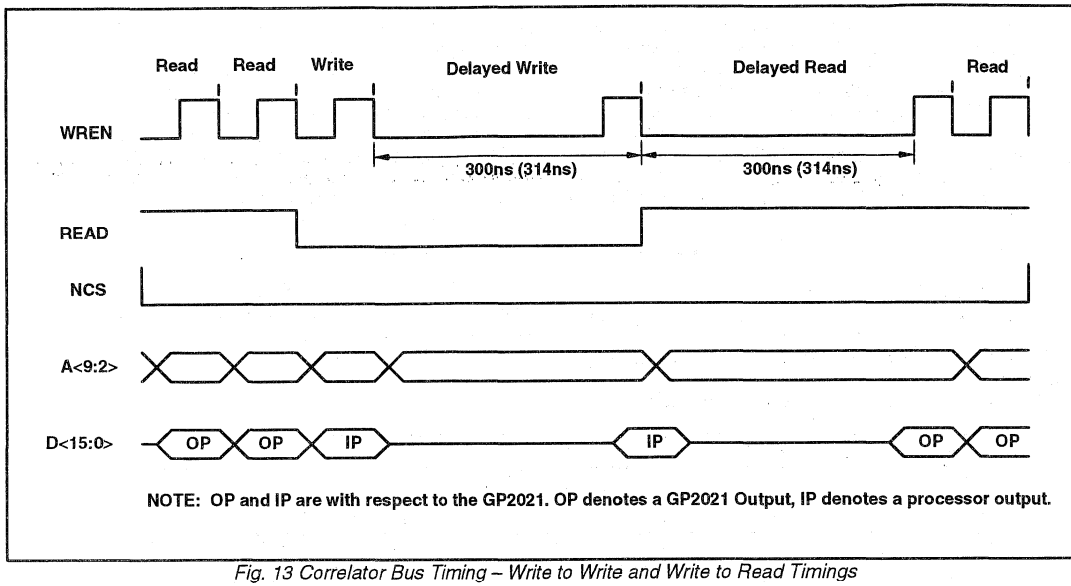


Fig. 13 Correlator Bus Timing – Write to Write and Write to Read Timings

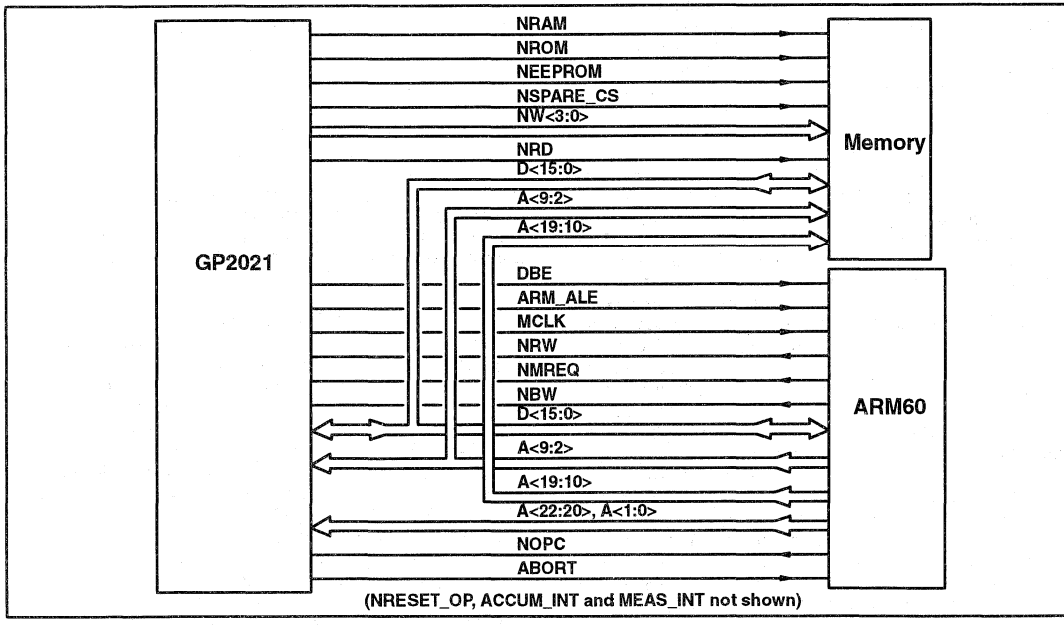


Fig. 14 : ARM System Mode

ARM System Mode

ARM System Mode, as shown in Fig 14, allows the GP2021 to be interfaced with an ARM60 microprocessor and external memory devices (i.e RAM, ROM, EEPROM, EPROM, Flash) without the need for external glue logic.

Address Map

Both the GP2021 and external memory devices are memory mapped into 1 Mbyte segments by A<22:20> as shown in Table 7.

A22	A21	A20	Device selected	Decoded output pin
0	0	0	ROM	NROM
0	0	1	RAM	NRAM
0	1	0	Correlator	
0	1	1	Support functions	
1	0	0	EEPROM	NEEPROM
1	0	1	User defined	NSPARE_CS
1	1	0	Not Decoded	
1	1	1	Not Decoded	

Table 7 ARM system map

The ARM60 is able to perform either byte or word (4 bytes wide) writes to memory. All registers within the GP2021 are word aligned, with only write accesses to external RAM being either byte or word aligned. The signal NBW is used to indicate either a byte or word write request, with A<1:0> performing byte selection.

Decoding of NBW and A<1:0> is performed by the Microprocessor Interface, with NW<3:0> being the byte write select outputs to memory. During a word write all four of the outputs NW<3:0> will be active.

Note that the register addresses for the Correlator and Support Functions are as shown in the GP2021 Register Map.

Control Signals

The GP2021 uses the ARM60 control signals NBW, NMREQ and NRW to generate the processor clock MCLK and the control signals ARM_ALE and DBE to match the timing requirements of the various memory devices .

The memory interface is via the memory chip select lines (NRAM, NEEPROM, NROM and NSPARE_CS) , the Read line (NRD) and the byte write select outputs (NW<3:0>).

ARM System Timing

The GP2021 timing diagrams for each of the memory interfaces (EEPROM, RAM, ROM, SPARE), and ARM60 are shown in the section Electrical Characteristics.

Wait State Generation

To allow access to slow peripherals or memory, the clock (MCLK) to the ARM60 microprocessor may be stretched in either Phase 1 (Low) or Phase 2 (High), thus allowing wait states to be introduced (where a wait state is defined as being one MCLK period long).

The GP2021 introduces one wait state for accesses to the Real Time Clock, Dual UART and System Control registers, as shown in Fig 15. Correlator accesses, as shown in Fig 19 incur one wait state; subsequent accesses being prevented from contravening the Correlator requirements (see Correlator Functional Description) by adding several wait states.

In order to ensure compatibility with a variety of memory devices, the ROM interface is programmable with between one to three wait states, while the EEPROM and SPARE interfaces can be programmed with between three to six wait states via the Wait State Register. For further information on the Wait State Register, refer to Detailed Description of Registers. Read and write cycles for the RAM, EEPROM (or Spare) and ROM interfaces are shown in Figs 16–18.

During a read cycle from Flash Memory, the output disable to data bus release time, could be greater than 25 ns. Hence in order to avoid bus contention, the nominal period of MCLK is stretched by 25 ns during the following cycle.

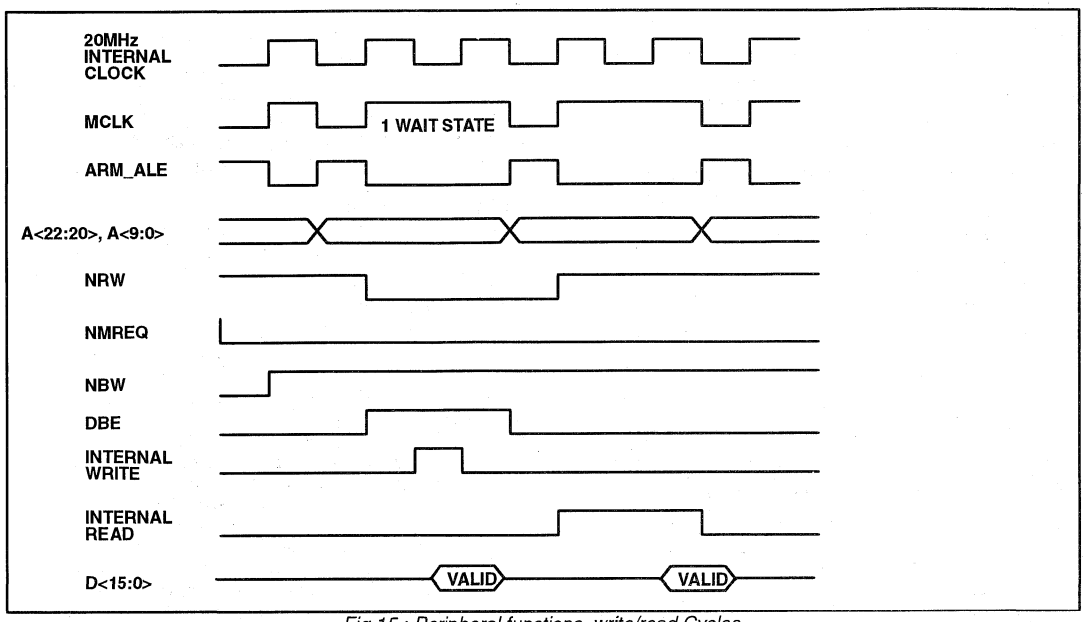


Fig.15 : Peripheral functions write/read Cycles.

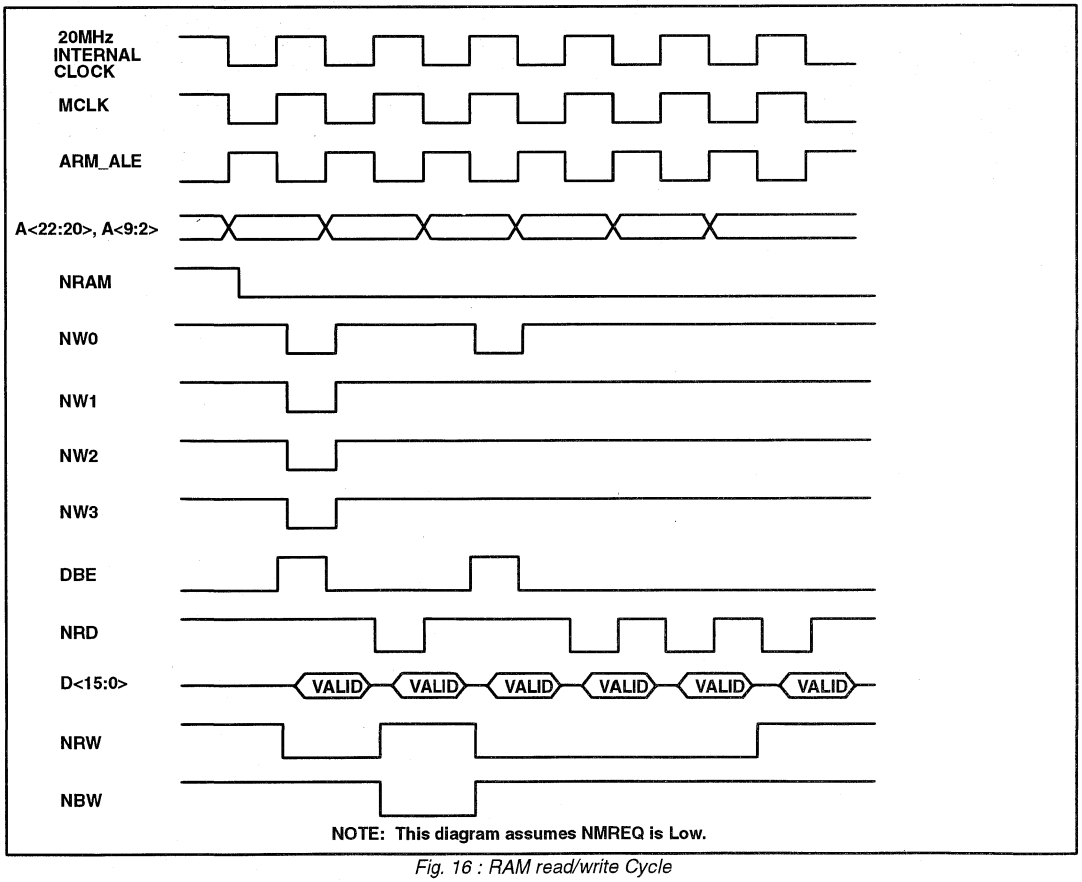


Fig. 16 : RAM read/write Cycle

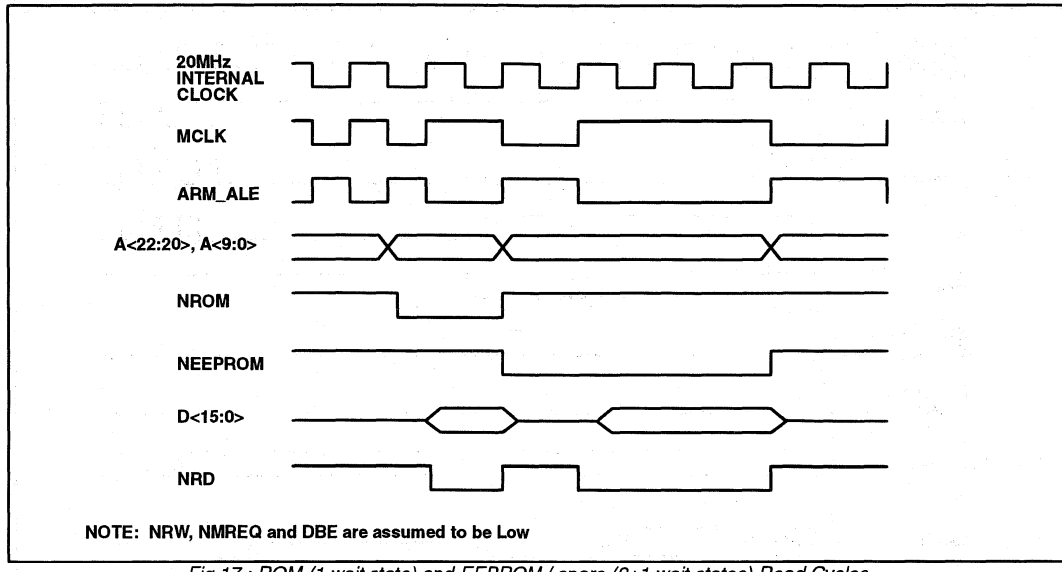


Fig.17 : ROM (1 wait state) and EEPROM / spare (2+1 wait states) Read Cycles

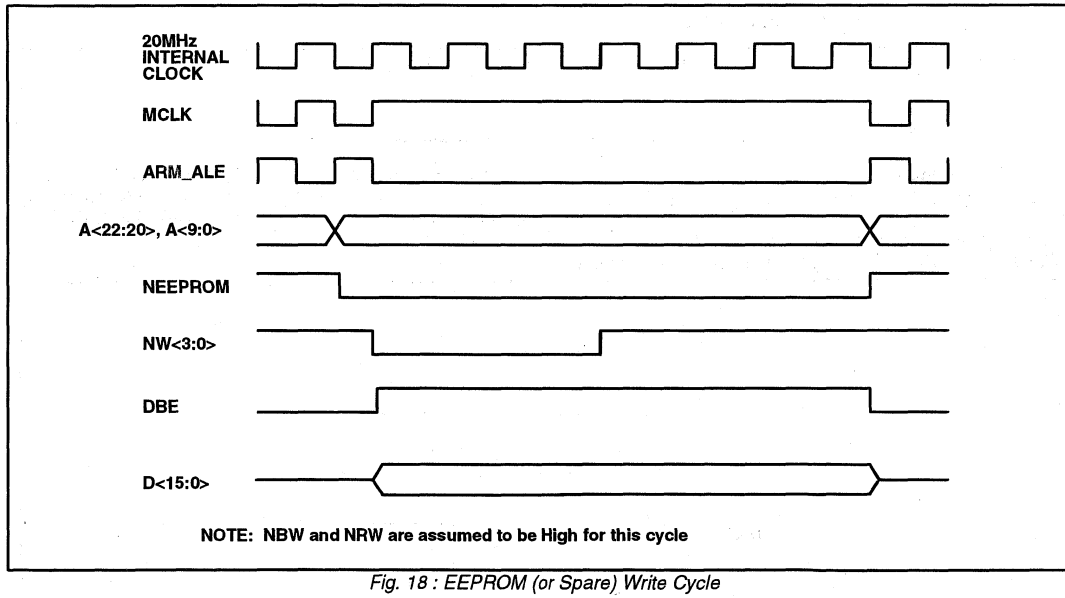


Fig. 18 : EEPROM (or Spare) Write Cycle

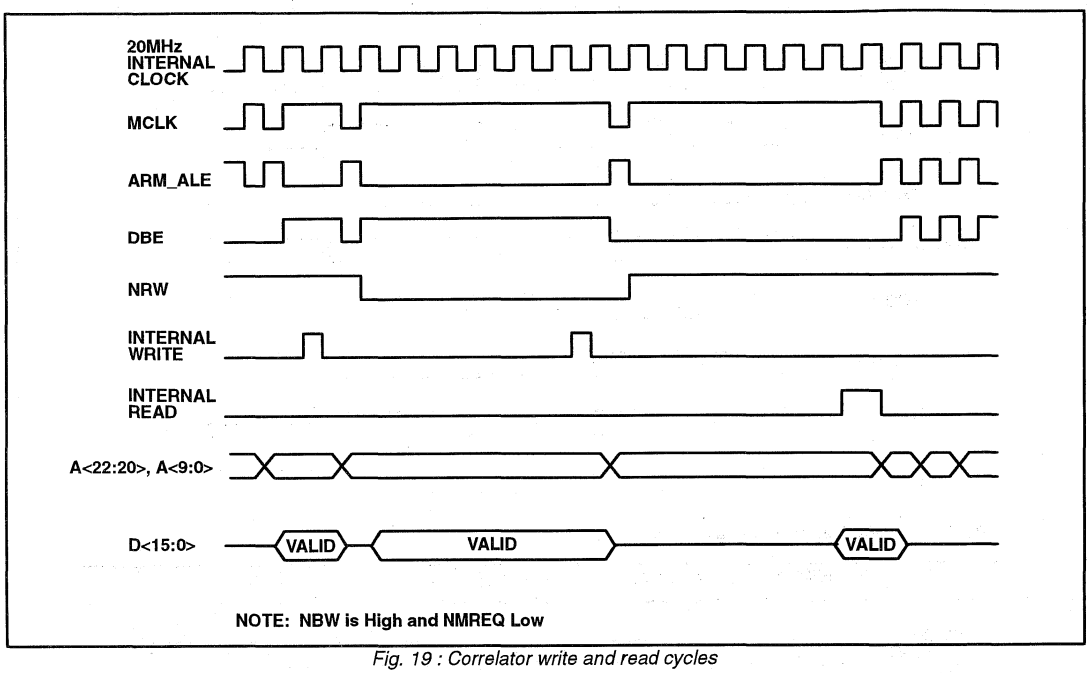


Fig. 19 : Correlator write and read cycles

Debug (Abort) Function

This is a feature designed to aid debugging and functions as follows:–
In ARM System Mode, the MULTI_FN_IO pin can be configured as a TRIGGER input to the Debug block via the IO_CONFIG register (see Detailed Description of Registers). In this mode a rising edge at the MULTI_FN_IO pin will generate a valid ARM data Abort sequence at the ABORT pin as shown in Fig. 20.

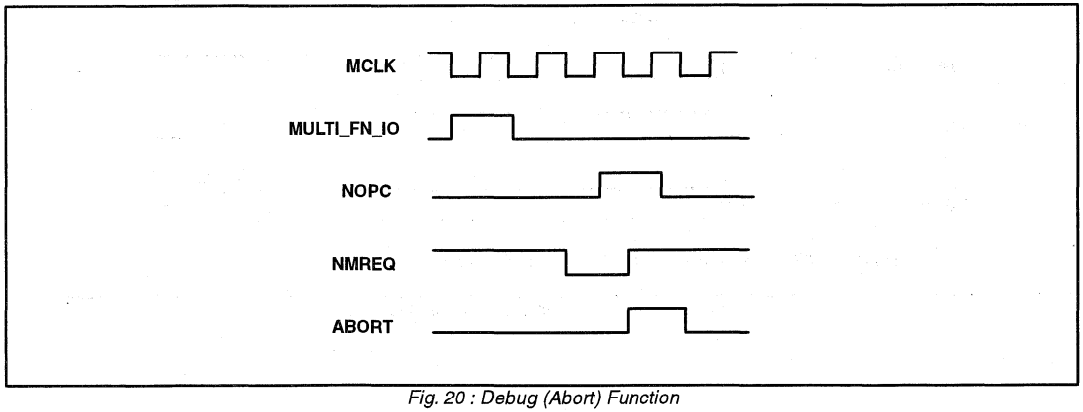


Fig. 20 : Debug (Abort) Function

Standard Interface Mode

This mode allows the GP2021 to be interfaced to most standard 16 and 32 bit microprocessors as shown in Fig. 21. No memory control is provided, so external glue logic may be required in order to interface the microprocessor to memory.

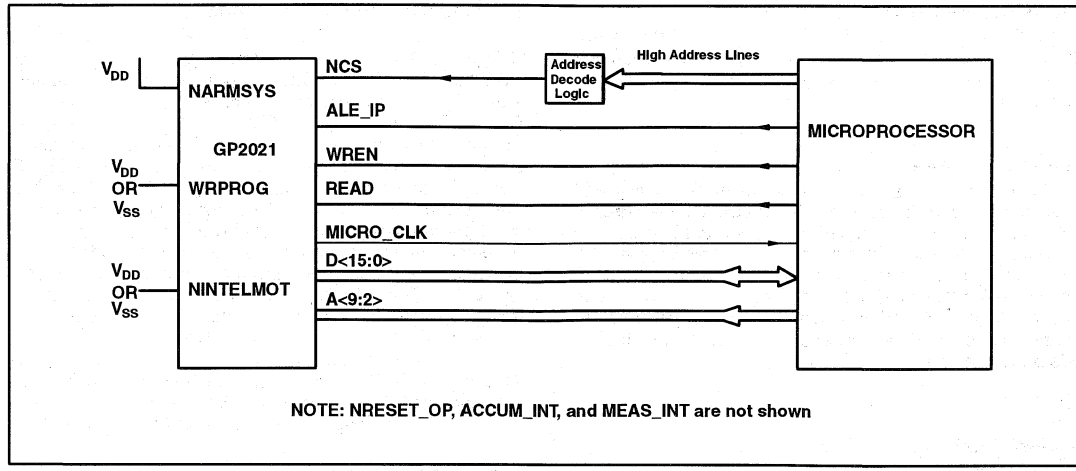


Fig. 21 : Standard Interface mode

Control Signals

In Standard Interface Mode (NARMSYS held high), the microprocessor interface of the GP2021 consists of two mode control pins, (NINTELMOT and WRPROG), and the control signals themselves, (ALE_IP, NCS, WREN and READ; the exact function of which is dependent upon the interface style selected).

Motorola Style Interface

(NINTELMOT = '1', WRPROG = 'X')

The WRPROG mode control pin is not used in Motorola Interface mode and should be tied High or Low. The ALE_IP (Address Latch Enable input) pin is used to transparently latch the address lines A<9:2> to the GP2021. If these address lines are already latched externally, this pin may be tied High. Note that the internal ALE signal is inhibited during a read or write strobe so the address lines may be changed once the read or write strobe has become active. The WREN pin acts as a WRITE/READ ENABLE strobe (active High) with the READ pin selecting either a READ strobe (READ = '1') or a WRITE strobe (READ = '0'). In a similar way to the addresses being latched during a read or write strobe, the READ signal is also latched during a data strobe and may be changed towards the end of the cycle.

The NCS pin is an active low chip select used to gate out the internal read and write strobes. In Standard Interface Mode, the GP2021 can best be visualised in terms of 3 signals, ALE_INT, WRSTROBE_INT and RDSTROBE_INT, the internal ALE, write strobe and read strobe signals. In Motorola Style Interface Mode these signals are derived as follows:

ALE_INT=ALE_IP. ($\overline{\text{WRSTROBE\_INT}}$ + $\overline{\text{RDSTROBE\_INT}}$)
WRSTROBE_INT = $\overline{\text{NCS}}$.WREN.$\overline{\text{READ}}$
RDSTROBE_INT = $\overline{\text{NCS}}$.WREN.READ

INTEL 80186 Style Interface

(NINTELMOT = '0', WRPROG = '0')

In the 80186 Style Interface mode the ALE_IP acts as an Address Latch Enable input (as in Motorola mode), used to transparently latch the address lines A<9:2> to the GP2021. Similar to Motorola mode, if the addresses are latched externally this pin may be tied High. Whereas Motorola mode used a single strobe input and a Read/$\overline{\text{Write}}$ level to denote read and write strobes, both INTEL modes use a pair of strobe inputs, one for reads, and one for writes. In this mode, READ acts as the active low read strobe (READ =$\overline{\text{RDSTROBE}}$) and WREN the active low write strobe (WREN= $\overline{\text{WRSTROBE}}$). NCS is the active low chip select used to gate out internal data strobes.

ALE_INT=ALE_IP
WRSTROBE_INT = $\overline{\text{NCS}}$.$\overline{\text{WREN}}$
RDSTROBE_INT = $\overline{\text{NCS}}$.$\overline{\text{READ}}$

INTEL 486 Style Interface

(NINTELMOT = '0', WRPROG='1')

The Intel 486 Style Interface is similar to the 80186 style interface, with similar separate read and write strobes. Some of the later Intel microprocessors (notably the i486) have a very small delay between the rising edge of ALE and the falling edge of the read or write strobes. Due to the pre–charged nature of the data–out bus of the Correlator, the address inputs must remain stable throughout the read strobe, and the small delay from ALE to read strobe would produce insufficient address setup times for correct operation. The 486 style interface mode removes this problem by gating both the read and write strobes such that they are inhibited until the falling edge of ALE_IP. The ALE_IP pin must not be tied High in 486 Style Interface mode.

ALE_INT= ALE_IP
WRSTROBE_INT = $\overline{\text{NCS}}$. $\overline{\text{WREN}}$. $\overline{\text{ALE\_IP}}$
RDSTROBE_INT = $\overline{\text{NCS}}$. $\overline{\text{READ}}$. $\overline{\text{ALE\_IP}}$

Reset

The NRESET_IP pin allows the GP2021 to be provided with an external system reset.
For further information refer to System Reset in Standard Interface Mode.

Register Addressing

As shown in the GP2021 Register Map, register addresses differ from those in ARM System Mode. In particular in Standard Interface Mode the GP2021 address bus interface is via A<9:2>, with NCS acting as its chip select input. The address pins A0, A1 in ARM System Mode now become the NRESET_IP and ALE_IP inputs. Hence, depending upon the system configuration employed, A<9:2> of the GP2021 could be connected to the microprocessor address pins A<7:0>.

CONTROLLING THE GP2021

The following section describes typical methods for controlling the GP2021. These include: signal acquisition and tracking, carrier phase measurement and timemark generation.

Search Operation

To perform signal acquistion, the carrier frequency and code phase space needs to be searched until the signal is detected. The maximum carrier frequency excursion from its nominal value is defined by the maximum carrier Doppler shift plus the maximum receiver clock error. The maximum code phase is defined by the (fixed) code length. Typically, all code phases will be searched at a given carrier frequency before advancing to the next carrier frequency bin and repeating the code phase search.

Carrier DCO Programming

The following registers:
CHx_CARRIER_DCO_INCR_HIGH
(or X_DCO _INCR_HIGH), and
CHx_CARRIER_DCO_INCR_LOW are programmed in sequence with the relevant data according to the frequency bin being searched. It is always necessary to write to both the _HIGH and _LOW registers. Carrier DCO programming will become effective as soon as the channel is released (made active). If the channel is already active, writes to CHx_CARRIER_DCO_INCR_LOW are effective immediately. (A small delay of up to 175ns will occur, to allow synchronisation of the processor write operation to the chip operation.)

Code DCO Programming

The CHx_CODE_DCO_INCR_HIGH
(or X_DCO_INCR_HIGH)
and the CHx_CODE_DCO_INCR_LOW registers are programmed in sequence with the relevant data according to the estimated code frequency offset. It is always necessary to write to both _HIGH and _LOW registers. Code DCO programming will become effective as soon as the channel is released (made active). If the channel is already active, writes to CHx_CODE_DCO_INCR_LOW are effective immediately. (A small delay of up to 175ns will occur to allow synchronisation of the processor write operation to the chip operation).

Code Generator Programming

For each channel, the CHx_SATCNTL register is programmed as follows:

(i) Set the SOURCESEL bit to select the input signal source.
(ii) Set the TRACK_SEL bits to set the Tracking arm code to either early or late (with respect to the Prompt arm).
(iii) Set the G2_LOAD bits to select the required PRN code.
(iv) Program the CHx_CODE_SLEW register with the desired code phase offset. The slew operation will become effective upon CHx_RSTB release. The first DUMP will generate accumulated data for the channel and set the associated CHx_NEW_ACCUM_DATA status bit.
(v) Release the relevant CHx_RSTB bits of the RESET_CONTROL register to make the channel active.

When the code clock is inhibited (to slew the code phase) the Integrate and Dump module is held reset. It will start to accumulate correlation results only after the slew operation is completed.

A search for a satellite on more than one channel may be performed using the MULTI channel addresses and different code slew values as appropriate.

Reading the Accumulated Data

At each DUMP the corresponding CHx_NEW_ACCUM_DATA status bit is set in the ACCUM_STATUS_A register. The status register, together with all accumulation registers (CHx_I_TRACK, CHx_Q_TRACK, CHx_I_PROMPT, CHx_Q_PROMPT) are mapped into consecutive addresses. These can be read as a consecutive block, if required, after every ACCUM_INT interrupt. Alternatively, the Status Registers may be polled. The Accumulation registers are not overwrite protected, therefore the system must respond quickly when new data becomes available. Whether or not it is necessary to process the accumulation at every DUMP is dependent upon the application. The order of reading them is optional, but ideally the CHx_Q_PROMPT register should be read last, because this resets the CHx_NEW_ACCUM_DATA bit.

The CHx_MISSED_ACCUM bits in the ACCUM_STATUS_B register indicate that new accumulated data has been missed. These can only be cleared by a write to CHx_ACCUM_RESET or by deactivating the channel.

Search on Other Code Phases

When it is desired to correlate on the next code phase, such as one whole chip later, the CODE_SLEW has to be programmed with a value of 2 (the units are half code chips). The slew will occur on the next DUMP. The effect of CODE_SLEW is relative to the current code phase. To repeat a CODE_SLEW, the register needs to be written to again even if the same size slew is required.

Once the signal has been detected (correlation threshold exceeded), the code and carrier tracking loops can be closed. The tracking loop parameters must be tailored in the software to suit the application.

Data Bit Synchronisation

The data bit synchronisation algorithm should find the data bit transition instant. The processor calculates the present one millisecond epoch and programs this value into the 1MS_EPOCH counter. Ideally, epoch counter accesses should occur following the reading of the accumulation register at each DUMP.

Alternatively, the epoch counters can be left free–running and the offset can be added by the software each time it reads the epoch registers. Note that if the integration is performed across bit boundaries, the integration result can be very small.

Reading the Measurement Data

At each TIC, the measurement data is latched in the Measurement Data registers
(CHx_EPOCH,
CHx_CODE_PHASE,
CHx_CARRIER_DCO_PHASE,
CHx_CARRIER_CYCLE_HIGH,
CHx_CARRIER_CYCLE_LOW,
CHx_CODE_DCO_PHASE).

The ACCUM_STATUS_B or MEAS_STATUS_A register must be polled at a rate greater than the TIC rate (to see if a TIC has occurred), otherwise measurement data will be lost. The ACCUM_INT or MEAS_INT events can be used to instigate this operation. The reading of measurement data can be either interrupt driven or polled. For the interrupt driven method the microprocessor reads the ACCUM_STATUS_B or MEAS_STATUS_A register after each MEAS_INT, and if the TIC bit is set, subsequently reads the Measurement data. For the polled method the ACCUM_STATUS_A register is always read following every ACCUM_INT. In addition the ACCUM_STATUS_B register is read on each ACCUM_INT to ensure no Accumulated Data has been missed and to check the TIC bit (along with several other status bits). The software tests the TIC bit to determine if new Measurement Data is available to be read.

Preset Mode

Each channel can be programmed into PRESET mode by writing a High into the PRESET/UPDATEB bit of the CHx_SATCNTL register.

When a TIC occurs, the satellite code, epoch value and slew numbers are loaded, and a new phase programmed into the Code DCO regardless of its previous value. Prior to the TIC the channel operates with its previous settings.

Preset Mode has no effect on the Carrier DCO and Carrier Cycle Counter.

If Preset mode is initiated, it should be allowed to operate to completion. The required sequence of operations is as follows:

(i) Write into CHx_SATCNTL to select the PRESET mode, together with the appropriate new settings.

ii) Load the Code and Carrier DCO increment values.

Note: These will take effect immediately thereby influencing the current measurements.

iii) Load the following Registers: CHx_CODE_DCO_PHASE, CHx_CODE_SLEW and CHx_EPOCH_COUNT_LOAD. It is important that the CHx_EPOCH_COUNT_LOAD occurs last, because it enables the preset operation on the next TIC.

Interrupts

There are 2 interrupt sources: ACCUM_INT and MEAS_INT. Their sense is dependant upon the selected microprocessor interface mode. The default ACCUM_INT period is 505.05µs. However, it can be reconfigured via the PROG_ACCUM_INT register or by changing the INTERRUPT_PERIOD or FRONT_END_MODE bits in the SYSTEM_SETUP register. The default MEAS_INT period is 50ms. However, this can be reconfigured via the PROG_TIC_HIGH and PROG_TIC_LOW registers.

Signal Path Delay Introduced by Hardware Signal Processing

When it is desired to generate an accurate time reference from GPS signals or to time–stamp position fixes the delays in the receiver must be allowed for. The signal path delay has two components, an Analogue path delay which varies with temperature and component tolerances; and a Digital path delay which is constant if oscillator drift variations are neglected.

The Digital delay is easier to estimate and is made up of the following:

In Real_Input mode:

(i) The time from the sampling edge of the SIGN and MAG bits in the front end (SAMPCLK) to the re–sampling in the Sample Latch (175 ns less the propagation delay of SAMPCLK to the Front–end).

(ii) Plus the time for the correlation in the Correlator on these same SIGN and MAG bits (125 ns).

(iii) Plus the delay in the accumulator to latch the sampled data (175 ns).

(iv) Less the time between the correlation and the TIC clock phase which is before the accumulator latch phase (75 ns), Giving a total of 400 ns less the SAMPCLK delay.

In Complex_Input mode:

(i) The time for the correlation in the Correlator on the SIGN and MAG bits after sampling (114 ns).

(ii) Plus the delay in the accumulator to latch the sampled data (171 ns).

(iii)Less the time between the correlation and the TIC clock phase which is before the accumulator latch phase (86 ns), giving a total of 199 ns.

The Analog delay through the radio receiver is set by such parameters as group delay in filters, which for the bandwidths used for C/A code will be in the region of 1 to 2 ms and so swamps the digital delay, but this can be measured and corrected for.

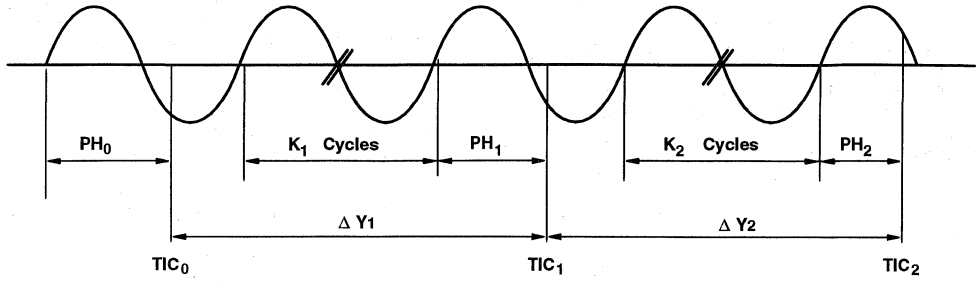
Integrated Carrier Phase Measurement

The Correlator tracking channel hardware allows measurement of integrated carrier phase through the CHx_CARRIER_CYCLE_HIGH and _LOW and the CHx_CARRIER_DCO_PHASE registers, which are part of the Measurement Data sampled at every TIC. The CHx_CARRIER_CYCLE_HIGH and _LOW registers contain the (20 bit) number of positive–going zero crossings of the Carrier DCO; this will be one more than the number of full cycles elapsed (4 bits are in _HIGH and 16 in _LOW register). The CHx_CARRIER_DCO_PHASE register contains the cycle fraction or phase, with 10 bit resolution to give 2π / 1024 radian increments.

To get the Integrated Carrier Phase over several TIC periods all that is needed is to read the CHx_CARRIER_CYCLE_HIGH and _LOW registers at every TIC and sum the readings. This gives a number 1 higher than the number of complete carrier cycles, when a carrier cycle is measured from one positive–going zero crossing to the next. To this number, the fractional carrier cycle at the end has to be added, and the fractional carrier cycle at the beginning has to be subtracted. Both numbers are read from the CHx_CARR_DCO_PHASE register. The total phase change can be calculated as follows :

Integrated Carrier Phase =
2π * Σ Numbers in Carrier Cycle Counter
+ final Carrier DCO phase
–Initial Carrier DCO phase

Fig. 22 shows how this equation is derived.



1. reading at TIC_0 : $CHx\_CARR\_DCO\_PHASE_0 = PH_0$
2. reading at TIC_1 : $CHx\_CARR\_DCO\_PHASE_1 = PH_1$
   $CHx\_CARR\_CYCLE_1 = K_1 + 1$
3. reading at TIC_2 : $CHx\_CARR\_DCO\_PHASE_2 = PH_2$
   $CHx\_CARR\_CYCLE_2 = K_2 + 1$

$$\Delta Y1 = 2\pi * K_1 + (2\pi - PH_0) + PH_1$$
$$= 2\pi(K_1 + 1) - PH_0 + PH_1$$
$$= 2\pi * (CHx\_CARR\_CYCLE_1 - CHx\_CARR\_DCO\_PHASE_0/1024 + CHx\_CARR\_DCO\_PHASE_1/1024)$$

$$\sum \Delta Y = 2\pi * (\sum_{i=1}^{last} CHx\_CARR\_CYCLE_i - CHx\_CARR\_DCO\_PHASE_0/1024 + CHx\_CARR\_DCO\_PHASE_{last}/1024)$$

Note: The Carrier Cycle Counter value is stored at every TIC and the Counter is reset

Fig. 22 : Integrated carrier phase

This Integrated Carrier Phase may be related to the delta–range, (the change in distance to each satellite). When used with the orbital parameters of the satellites, the delta–ranges give a measure of the receiver's movement between fixes, which is independent of those fixes and so can be used to smooth them. It can also give a velocity directly. The delta–ranges will be noisy and most of the value is due to satellite movement so the determination of velocity must use data from adequately separated TICs. For position smoothing all delta–ranges may be included in the input to the navigation filter, as that filter will perform a running average of the delta–ranges as well as the ranges.

Timemark Generation

The GP2021 is capable of generating an accurate TIMEMARK timing output on one of the discrete outputs if required. TIMEMARK is intended to be a UTC aligned timing output with an accurate 1 second period and a pulse width of 1ms. The TIMEMARK output is always derived from a rising edge on TIC, and for UTC aligned operation the TIC counter must be brought into phase with UTC. This is done by modifying the division ratio of the TIC counter for a single TIC period, by increasing or reducing the division ratio, thus slewing the phase of TIC. Since the TIC counter is incremented every 175ns which is not an exact sub–multiple of 1 second it is also necessary to continually monitor the relationship between TIC and UTC to keep TIC in phase with UTC. Once TIC is in phase with UTC, the TIMEMARK output can be derived from TIC using one of 2 methods both of which involves writing to TIMEMARK_CONTROL: (1) The GP2021 can be armed to produce a TIMEMARK output at the next TIC only, or (2) It can be programmed to give a TIMEMARK output every n TICs starting at the next TIC.

A separate counter resets the TIMEMARK output giving a 1ms pulse width. The TIC counter can be programmed with an accuracy of 175ns in Real_Input mode or 171.4ns in Complex_Input mode. This determines the accuracy of the TIMEMARK output. If the TIC is continually synchronised to keep the rising edge as close as possible to UTC, the internal TIMEMARK will be within 100ns (4/7 x 175ns) of UTC in Real_Input mode or 85.7ns (3/6 x 171.4ns) of UTC in Complex_Input mode. In addition, there may be a delay of up to 50ns in getting the TIMEMARK output off chip, giving a maximum error of 150ns (Real_Input) or 135.7ns (Complex_Input) between TIMEMARK and UTC. It should be noted that due to the need to re–synchronise TIC, a jitter of up to 175ns may be present on TIMEMARK, along with any jitter and drift present on the input clock. The pulse width of TIMEMARK (in seconds) is either (5714 + 2/7) * (7/ Master Clock Frequency) for Real_Input mode giving 1.0000000ms (assuming an accurate 40MHz master clock input) or (5833 + 1/6) * (6 / Master Clock Frequency) for Complex_Input mode giving 0.9999714ms (assuming an accurate 35MHz master clock input).

DETAILED DESCRIPTION OF REGISTERS

GP2021 Register Map

The register map of the GP2021 is shown below. The addresses are complete, and it should be noted that all the register addresses are word–aligned, i.e. A0 and A1 are not used. Adjacent register addresses thus increment by 4, in ARM System Mode. However, in Standard Interface Mode, the GP2021 address lines A<9:2> could be connected to the processor address lines A<7:0>. Note that in this mode pins A0 and A1 are allocated other functions.

REGISTER BLOCK		ADDRESS (Hex) ARM SYSTEM MODE A<22:20>	A<9:0>	ADDRESS (Hex) STANDARD INTERFACE MODE A<9:2>	REGISTERS
CORRELATOR					
	CNTL	2	000 to 01C	00 to 07	CH0 Control
	CNTL	2	020 to 03C	08 to 0F	CH1 Control
	CNTL	2	040 to 05C	10 to 17	CH2 Control
	CNTL	2	060 to 07C	18 to 1F	CH3 Control
	CNTL	2	080 to 09C	20 to 27	CH4 Control
	CNTL	2	0A0 to 0BC	28 to 2F	CH5 Control
	CNTL	2	0C0 to 0DC	30 to 37	CH6 Control
	CNTL	2	0E0 to 0FC	38 to 3F	CH7 Control
	CNTL	2	100 to 11C	40 to 47	CH8 Control
	CNTL	2	120 to 13C	48 to 4F	CH9 Control
	CNTL	2	140 to 15C	50 to 57	CH10 Control
	CNTL	2	160 to 17C	58 to 5F	CH11 Control
	CNTL	2	180 to 19C	60 to 67	MULTI Control
		2	1A4	69	X_DCO_INCR_HIGH
		2	1AC	6B	PROG_ACCUM_INT
		2	1B4	6D	PROG_TIC_HIGH
		2	1BC	6F	PROG_TIC_LOW
	CNTL	2	1C0 to 1DC	70 to 77	ALL Control
		2	1EC	7B	TIMEMARK_CONTROL
		2	1F0	7C	TEST_CONTROL
		2	1F4	7D	MULTI_CHANNEL _SELECT
		2	1F8	7E	SYSTEM_SETUP
		2	1FC	7F	RESET_CONTROL
		2	200 to 20C	80 to 83	Status Registers
	ACCUM	2	210 to 21C	84 to 87	CH0 Accumulate
	ACCUM	2	220 to 22C	88 to 8B	CH1 Accumulate
	ACCUM	2	230 to 23C	8C to 8F	CH2 Accumulate
	ACCUM	2	240 to 24C	90 to 93	CH3 Accumulate
	ACCUM	2	250 to 25C	94 to 97	CH4 Accumulate
	ACCUM	2	260 to 26C	98 to 9B	CH5 Accumulate
	ACCUM	2	270 to 27C	9C to 9F	CH6 Accumulate
	ACCUM	2	280 to 28C	A0 to A3	CH7 Accumulate
	ACCUM	2	290 to 29C	A4 to A7	CH8 Accumulate
	ACCUM	2	2A0 to 2AC	A8 to AB	CH9 Accumulate
	ACCUM	2	2B0 to 2BC	AC to AF	CH10 Accumulate
	ACCUM	2	2C0 to 2CC	B0 to B3	CH11 Accumulate
	ACCUM	2	2D0 to 2DC	B4 to B7	MULTI Accumulate
	ACCUM	2	2E0 to 2EC	B8 to BB	ALL Accumulate

REGISTER BLOCK	ADDRESS (Hex) ARM SYSTEM MODE A<22:20>	A<9:0>	ADDRESS (Hex) STANDARD INTERFACE MODE A<9:2>	REGISTERS
REAL – TIME CLOCK				
	3	000	C0	RTC_LS
	3	004	C1	RTC_2ND
	3	008	C2	RTC_MS
	3	00C	C3	CLOCK_RESET
	3	010	C4	WATCHDOG_RESET
DUART				
	3	040	D0	TX_DATA_A, RX_DATA_A
	3	044	D1	TX_DATA_B, RX_DATA_B
	3	048	D2	CONFIG_A, STATUS_A
	3	04C	D3	CONFIG_B, STAUS_B
	3	050	D4	RESET_A
	3	054	D5	RESET_B
	3	058	D6	TX_RATE_A
	3	05C	D7	TX_RATE_B
SYSTEM CONTROL				
	3	080	E0	WAIT_STATE
	3	084	E1	SYSTEM_CONFIG
	3	088	E2	Not Used
	3	08C	E3	SYSTEM_ERROR_STATUS
	3	090	E4	DATA_RETENT
GENERAL CONTROL				
	3	0C0	F0	IO_CONFIG
	3	0C4	F1	TEST_CONFIG
	3	0C8	F2	DATA BUS TEST

Table 8: GP2021 Register Map

Correlator Registers

Addresses for the Correlator Registers may be calculated from a base address with an increment for a particular register.

The base addresses for the CNTL and ACCUM register blocks for each channel in the Correlator are shown in the GP2021 Register Map, the increments being given below:

eg. CH3_CODE_DCO_INCR_LOW = 060H + 018H = 078H

Tracking Channel Registers

ADDRESS (Hex)		WRITE FUNCTION	READ FUNCTION
ARM SYSTEM MODE	STANDARD INTERFACE MODE		
CNTL + 00	CNTL + 0	SATCNTL	CODE_SLEW
+ 04	+ 1	CODE PHASE COUNTER *	CODE_PHASE
+ 08	+ 2	CARRIER_CYCLE_COUNTER *	CARRIER_CYCLE_LOW
+ 0C	+ 3	CARRIER_DCO_INCR_HIGH	CARRIER_DCO_PHASE
+ 10	+ 4	CARRIER_DCO_INCR_LOW	EPOCH (Latched)
+ 14	+ 5	CODE_DCO_INCR_HIGH	CODE_DCO_PHASE
+ 18	+ 6	CODE_DCO_INCR_LOW	CARRIER_CYCLE_HIGH
+ 1C	+ 7	EPOCH_COUNT_LOAD	EPOCH_CHECK (Not latched)
ACCUM + 00	ACCUM + 0	CODE_SLEW_COUNTER	I_TRACK
+ 04	+ 1	ACCUM_RESET	Q_TRACK
+ 08	+ 2	not used	I_PROMPT
+ 0C	+ 3	CODE_DCO_PRESET_PHASE	Q_PROMPT

NOTE: The registers labelled * (the CODE_PHASE_COUNTER and CARRIER_CYCLE_CONTROL) can only be written to if 'Test' mode has been selected by setting bit 3 of the TEST CONTROL register to High.

ADDRESS (HEX)		WRITE FUNCTION	READ FUNCTION
ARM SYSTEM MODE	STANDARD INTERFACE MODE		
200	80	STATUS	ACCUM_STATUS_C
204	81	not used	MEAS_STATUS_A
208	82	not used	ACCUM_STATUS_A
20C	83	not used	ACCUM_STATUS_B

In both the ACCUM and CNTL sections there are some addresses labelled ALL or MULTI in place of CHx. Writing to these addresses will write to all channels or to a selection set by MULTI_CHANNEL_SELECT in one operation and so may be used to initialise the system quickly or to load the next search settings with little bus use. This is a write only function and the corresponding CHx read functions are not available at addresses labelled ALL or MULTI.

It can be seen that the addresses in CNTL are used to control the device in write mode but give the Measurement Data when in read mode.

Apart from the Code and Carrier DCO increment values, all data transfers are only 16 bit wide. Writes to the Code and Carrier DCO's are 32 bit data transfers where the _HIGH word should be written first and will be retained in the 16 to 32 bit interface until the _LOW word is written, which must occur as the next write to the chip. All 32 bits will then be transferred into the DCO increment register. Data is written to an input buffer in the 16 to 32 bit interface and will be transferred to its destination register during the next full cycle of the 7 (or 6) phase clock. Write cycles should therefore have a period of at least 300 ns. The X_DCO_INCR_HIGH may be used to write the high bits of the increment number to any or all DCO's as an alternative to using the CHx_CODE/CARRIER_DCO_INCR–_HIGH addresses. By using this address, there is no need to wait 300ns before writing the _LOW part. For further information refer to General Interface Timing in Microprocessor Interface section.

The bit assignments for the Correlator registers are given below, but two write–only registers do not have any data bits, these are:

(1) A write to the CHx_ACCUM_RESET register (irrespective of what data is written) will reset the ACCUM_STATUS_A, ACCUM_STATUS_B, and ACCUM_STATUS_C registers for that channel.
(2) A write to the STATUS register (irrespective of what data is written) will latch the state of the various status flags into ACCUM_STATUS_A,
ACCUM_STATUS_B,
ACCUM_STATUS_C
Registers for all channels. This allows a polling based rather than Interrupt driven tracking scheme.

The registers are listed in alphabetical order and not in address order to allow easy reference to each section. Unless otherwise stated the LSB is bit 0 and the MSB is bit 15 or as far up the register as there is data. Note that most registers do not have both read and write functions, and many addresses are shared between read–only and write–only registers having different functions.

ACCUM_STATUS_A (Read Address)

Bit	Bit Name
15	ACCUM_INT
14	Not used –LOW
13	Not used –LOW
12	Not used –LOW
11	CH11_NEW_ACCUM_DATA
10	CH10_NEW_ACCUM_DATA
9	CH9_NEW_ACCUM_DATA
8	CH8_NEW_ACCUM_DATA
7	CH7_NEW_ACCUM_DATA
6	CH6_NEW_ACCUM_DATA
5	CH5_NEW_ACCUM_DATA
4	CH4_NEW_ACCUM_DATA
3	CH3_NEW_ACCUM_DATA
2	CH2_NEW_ACCUM_DATA
1	CH1_NEW_ACCUM_DATA
0	CH0_NEW_ACCUM_DATA

ACCUM_STATUS_A is a register containing the state of twelve status bits sampled and latched on the active edge of every ACCUM_INT. They can also be sampled and latched on request, by performing a write operation to STATUS. (This is safe only if the interrupts are stopped, by setting INTERRUPT_ENABLE bit to LOW in the SYSTEM_SETUP register.) The microprocessor must respond to each ACCUM_INT and read the channel registers before the next DUMP is due in that channel.

The ACCUM_INT bit is set HIGH at every ACCUM_INT and is reset by reading the ACCUM_STATUS_A register. This status bit is reset by a hardware master reset but not by a software reset (MRB).

The CHx_NEW_ACCUM_DATA status bit indicates that a DUMP has occurred in that channel, and that new Accumulated Data is available to be read.

Each bit is cleared by the trailing edge of a read of the associated CHx_Q_PROMPT register or by a write to CHx_ACCUM_RESET.

Note that the channel specific bits of this register will not show their new value until after an active edge of ACCUM_INT or a write to the STATUS register. Disabling a channel will however, clear the bit immediately.

ACCUM_STATUS_B (Read Address)

Bit	Bit Name
15	DISCIP_GLITCH
14	DISCIP
13	TIC
12	MEAS_INT
11	CH11_MISSED_ACCUM
10	CH10_MISSED_ACCUM
9	CH9_MISSED_ACCUM
8	CH8_MISSED_ACCUM
7	CH7_MISSED_ACCUM
6	CH6_MISSED_ACCUM
5	CH5_MISSED_ACCUM
4	CH4_MISSED_ACCUM
3	CH3_MISSED_ACCUM
2	CH2_MISSED_ACCUM
1	CH1_MISSED_ACCUM
0	CH0_MISSED_ACCUM

The lower 12 bits of ACCUM_STATUS_B bits are sampled and latched on the active edge of every ACCUM_INT signal. They can be sampled and latched on request by performing a write operation to STATUS (as with ACCUM_STATUS_A).

The DISCIP_GLITCH bit will be set High if a glitch to Low has occurred on the DISCIP pin since the last read of this register. It is cleared by reading this ACCUM_STATUS_B register. This bit is reset by a hardware master reset (RESETB at Low) but not by a software reset. The minimum reliably detectable glitch width is 25ns.

The DISCIP bit indicates the level on the DISCIP input pin at the time this read occurs and may be used to interface a hardware condition (such as a ready flag from a UART or the PLL LOCK signal from a front–end) to the microprocessor without using an interrupt. This bit is not reset by a hardware master reset nor by an MRB.

The TIC bit is set High at every TIC and is cleared by reading this ACCUM_STATUS_B register. Its purpose is to tell the microprocessor that new Measurement Data is available. It is reset by a hardware master reset (RESETB at Low) but not by an MRB in RESET_CONTROL.

Provided that interrupts are enabled, the MEAS_INT bit is set High at each TIC and 50 ms before each TIC (if the TIC period is greater then 50 ms), and is cleared by reading this register. This bit can be used as a flag to the microprocessor, to time software module swapping. It is reset by a hardware master reset (RESETB at Low), but not by a software reset.

CHx_MISSED_ACCUM status bit indicates (when High) that there has been missed Accumulated Data due to a new DUMP in CHx before the previous data has been read. This bit is latched until the associated CHx_ACCUM_RESET is written to. If any data is missed due to the reading process being too slow this must be allowed for in the software, such as by checking the Navigation Message data bit transitions independently of the sets of Accumulated Data reads. If too much data is lost the system signal to noise ratio will be degraded. The primary purpose of these bits is as a check on how well the tracking routines are working – once the whole design is complete these bits should not become set.

Note that the channel specific bits of this register will not show their new value until after an active edge of ACCUM_INT or a write to the STATUS register. Disabling a channel will however, clear the bit immediately.

ACCUM_STATUS_C (Read Address)

Bit	Bit Name
15	not used – LOW
14	not used – LOW
13	not used – LOW
12	not used – LOW
11	CH11_EARLY_LATEB
10	CH10_EARLY_LATEB
9	CH9_EARLY_LATEB
8	CH8_EARLY_LATEB
7	CH7_EARLY_LATEB
6	CH6_EARLY_LATEB
5	CH5_EARLY_LATEB
4	CH4_EARLY_LATEB
3	CH3_EARLY_LATEB
2	CH2_EARLY_LATEB
1	CH1_EARLY_LATEB
0	CH0_EARLY_LATEB

ACCUM_STATUS_C bits are sampled and latched on the active edge of every ACCUM_INT signal, or they can be sampled and latched on request by performing a write operation to STATUS (as with ACCUM_STATUS_A).

CHx_EARLY_LATEB status bit indicates the code type for the Accumulated Data on the Tracking arm of channel CHx when that channel is in Dithering mode. A High indicates an EARLY code and a Low indicates a LATE code. Each individual bit is determined on the DUMP that sets CHx_NEW_ACCUM_DATA to High for that channel. In other modes the bit is of no use.

Note that the channel specific bits of this register will not show their new value until after an active edge of ACCUM_INT or a write to the STATUS register. Disabling a channel will however, clear the bit immediately.

CHx_ACCUM_RESET

(Write Address)

Bits 15 to 0: Not used.

These are write–only locations provided to allow resetting of the status bits ACCUM_STATUS_A, ACCUM_STATUS_B, and ACCUM_STATUS_C associated with a given channel or all channels. When these locations are written to, the data is irrelevant.

CHx_CARRIER_CYCLE_COUNTER, MULTI_CARRIER_CYCLE_COUNTER, ALL _CARRIER_CYCLE_COUNTER

(Write Address)

A write to these registers only has effect when in test mode (bit 3 of TEST_CONTROL set High). The value on the bus is loaded into the lower 16 bits of the CHx_CARRIER_CYCLE_COUNTER along with zeros into the upper 4 bits.

CHx_CARRIER_CYCLE_HIGH, CHx_CARRIER_CYCLE_LOW

(Read Address)

_HIGH bits 15 to 4 : not used – LOW when read.
_HIGH bits 3 to 0: Carrier Cycle Count bits 19 to 16.
_LOW bits 15 to 0: Carrier Cycle Count bits 15 to 0.

The Correlator tracking channel hardware allows for measurement of integrated carrier phase through the CHx_CARRIER_CYCLE_HIGH and _LOW and the CHx_CARRIER_DCO_PHASE registers, which are part of the Measurement Data sampled at every TIC. The CHx_CARRIER_CYCLE_HIGH and _LOW registers contain the 20 bit number of positive going zero crossings of the Carrier DCO (4 bits are in _HIGH and 16 in _LOW).
The cycle fraction can be read from the CHx_Carrier_DCO_Phase register.

In the CHx_CARRIER_CYCLE counter, a TIC generates two consecutive actions. First it latches the 4 more significant bits of the cycle counter into CHx_CARRIER_CYCLE_HIGH and the 16 less significant bits into CHx_CARRIER_CYCLE_LOW. Then it resets the cycle counter.

After each TIC, every time the Carrier DCO accumulator generates an overflow as a result of a carrier cycle being completed, the cycle counter increments by one.

In Real_Input mode the nominal CARRIER DCO frequency with no Doppler and no oscillator drift compensation is 1·405396825 MHz, so in 100 ms, there will be about 140540 cycles.

In almost all applications the number of Carrier DCO cycles does not vary much from one TIC interval to another so it is possible to predict the Most Significant Bits of the value, and then only read the CHx_CARRIER_CYCLE_LOW register.

CHx_CARRIER_CYCLE_HIGH and _LOW contents are not protected by an overwrite protection mechanism and so must be read before the next TIC.
For further information on the Carrier Cycle Counter refer to Detailed Operation of GP2021.*

* Refer to page 9.

CHx_CARRIER_DCO_INCR_HIGH, X_DCO_INCR_HIGH, MULTI_CARRIER_DCO_INCR_HIGH, ALL_CARRIER_DCO_INCR_HIGH, CHx_CARRIER_DCO_INCR_LOW, MULTI_CARRIER_DCO_INCR_LOW, ALL_CARRIER_DCO_INCR_LOW

(Write Address)

_INCR_HIGH bits 15 to 10: Not used in this operation.
_INCR_HIGH bits 9 to 0 : More significant bits (25 to 16) of the Carrier DCO phase increment when used before a write to _CARRIER_DCO_INCR_LOW.
_INCR_LOW bits 15 to 0 : Less significant bits (15 to 0) of the Carrier DCO phase increment.

The contents of registers _INCR_HIGH and_INCR_LOW are combined to form the 26 bits of the CHx_CARRIER_DCO_INCR register, the carrier DCO phase increment number. In order to write successfully, the top 10 bits must be written first, to any of the _HIGH addresses. They will be stored in a buffer and only be transferred into the increment register of the DCO together with the _LOW word. A 26 bit increment number is adequate for a 27 bit accumulator DCO, as the increment to the MSB is always zero.

The LSB of the INCR register represents a step given by :

Min Step Frequency = $(40MHz/7)/2^{27}$
(in Real_Input mode) = 42.57475mHz

Min Step Frequency = $(35MHz/6)/2^{27}$
(in Complex_Input mode) = 43.46172mHz

The output Frequency = CHx_CARRIER_DCO_INCR * Min Step Frequency.

With a GP2015/GP2010 style front end, the nominal value of the IF is 1.405396826 MHz before allowing for Doppler shift or crystal error. Writing 01F7B1B9H into the CHx_CARRIER_DCO_INCR register will generate a local oscillator frequency of 1.405396845 MHz.

CHx_CARRIER_DCO_PHASE

(Read Address)

Bits 15 to 10: Not used – Low when read.
Bits 9 to 0: More significant bits (26 to 17) of CHx_CARRIER_DCO_PHASE as sampled at the last TIC. The weight of the least significant bit is 2π / 1024 radians of a Carrier DCO cycle. These bits form an unsigned integer valid from 0 to 1023. CHx_CARRIER_DCO_PHASE provides sub–cycle phase measurement information and so complements the information given by CHx_CARRIER_CYCLE_HIGH and _LOW.

The register value is latched on each TIC and is not protected by any overwrite protection mechanism.

CHx_CODE_DCO_INCR_HIGH, X_DCO_INCR_HIGH, MULTI_CODE_DCO_INCR_HIGH, ALL_CODE_DCO_INCR_HIGH, CHx_CODE_DCO_INCR_LOW, MULTI_CODE_DCO_INCR_LOW, ALL_CODE_DCO_INCR_LOW

(Write Address)

_INCR_HIGH bits 15 to 9: Not used in this operation.
_INCR_HIGH bits 8 to 0: More significant bits (24 to 16) of the Code DCO phase increment when used before a CODE_DCO_INCR_LOW.

_INCR_LOW bits 15 to 0: Less significant bits (15 to 0) of the Code DCO phase increment.

The contents of registers _INCR_HIGH and _INCR_LOW are combined to form the 25 bits of the CHx_CODE_DCO_INCR register, the Code DCO phase increment number. In order to write successfully, the top 9 bits must be written first, to any of the _HIGH addresses. They will be stored in a buffer and only be transferred into the increment register of the DCO together with the _LOW word. A 25 bit increment number is adequate for a 26 bit accumulator DCO as the increment to the MSB is always zero.

The LSB of the INCR register represents a step given by:

Min Step Frequency = (40MHz/7)/2^{26}
(in Real_Input mode) = 85.14949mHz

Min Step Frequency = (35MHz/6)/2^{26}
(in Complex_Input mode) = 86.92344mHz

The output Frequency = CHx_CODE_DCO_INCR * Min Step Frequency.

Note: The Code DCO drives the Code Generator to give half–chip time steps and so must be programmed to twice the required chip rate. This means that the chip rate resolution is 42·57475mHz in Real_Input mode or 43.46172mHz in Complex_mode.

The nominal frequency is 1.023000000 MHz before allowing for Doppler shift or crystal error. Writing 016EA4A8H into the CHx_CODE_DCO_INCR register will generate a chip rate of 1.022999968 MHz in Real_Input mode. In Complex_mode, 01672922H will generate a chip rate of 1.022999970 MHz.

CHx_CODE_DCO_PHASE

(Read Address)

Bits 15 to 10: Not used, (Low when read).
Bits 9 to 0: CHx_CODE_DCO_PHASE: Contains the ten more significant bits (25 to 16) of the Code DCO phase accumulator sampled at a TIC event. It is an unsigned integer valid from 0 to 1023. The weight of the least significant bit is $2\pi/1024$ radians, 2π being half of a code chip, so the pseudorange resolution is 1/2048 of a chip, (equivalent to 0·15 metre or 0·5 ns).

The CHx_CODE_DCO_PHASE content is not protected by any overwrite protection mechanism.

CHx_CODE_DCO_PRESET_PHASE, MULTI_CODE_DCO_PRESET_PHASE, ALL_CODE_DCO_PRESET_PHASE

(Write Address)

Bits 15 to 8: Not used.
Bits 7 to 0: More significant bits (25 to 18) of the Code DCO phase which is to be loaded at the next TIC event in PRESET mode.

In PRESET mode, the 8 bits of the CHx_CODE_DCO_PRESET_PHASE register, with zeros filling the lower bits, are transferred to the CODE DCO accumulator on the next TIC. The previous accumulator phase is totally overwritten. The PRESET_PHASE register is a write–only register and it can be written to at any time in PRESET mode or in UPDATE mode, but only has effect when PRESET mode is entered. The weight of the least significant bit of PRESET phase is 2π / 256 radians of a half chip cycle.

In UPDATE mode this register has no use other than as preparation for PRESET mode.

Refer to Detailed Operation of GP2021 for further information on PRESET mode. *

* Refer to page 9.

CHx_CODE_PHASE (Read Address) CHx_CODE_PHASE_COUNTER, MULTI_CODE_PHASE_COUNTER, ALL_CODE_PHASE_COUNTER

(Write Address)

Bits 15 to 11: Not used, Low when read.
Bits 10 to 0: CHx_CODE_PHASE (Read) – This is the state of the Code Phase Counter, (an 11–bit binary up counter clocked by the Code Generator Clock), stored on TIC. The phase is expressed as a number of half code chips and ranges from 0 to 2046 half chips. A reading of 2046 is very rare and can only occur if the TIC captures the Code phase just after the counter reaches 2046 and before it is reset by a DUMP from the C/A Code Generator. DUMP also increments the Epoch counter, so the meaning of a phase value of 2046 + the previous Epoch value is the same as a phase value of 0 + the incremented Epoch value, and either is valid. If a TIC occurs during a Code Slew the reading will be 0, and that channel's Measurement Data is of no use.
Bits 10 to 0: (Write) loads the 11 bits of the CHx_CODE_PHASE_COUNTER. A write to these registers is only possible in test mode, enabled by setting the TM_TEST (bit of TEST_CONTROL) to High.

CHx_CODE_SLEW (Read Address) CHx_CODE_SLEW_COUNTER, MULTI_CODE_SLEW_COUNTER, ALL_CODE_SLEW_COUNTER

(Write Address)

Bits 15 to 11: Not used.
Bits 10 to 0 : An unsigned integer ranging from 0 to 2047 representing the number of code half chips to be slewed immediately after the next DUMP if in UPDATE mode or after the next TIC, if in PRESET mode. Since there are only 2046 half chips in a GPS C/A code, a programmed value of 2047 is equivalent to a programmed value of 1, but the next DUMP event will take place 1 ms later. In PRESET mode, the slew timing is set only by TIC, which will also reset the code generator, (no DUMP is needed). A non–zero slew must always be programmed when using PRESET mode.

The CHx_CODE_SLEW register can be written to at any time. If two accesses have taken place before a DUMP in UPDATE mode or before a TIC when in PRESET mode, the latest value will be used at the next slew operation. During the time a slew process is being executed, any further write access to the CHx_CODE_SLEW register will be stored until the following DUMP and then cause the transfer of this new value into the counter. This situation may be avoided by synchronising the access with the associated CHx_NEW_ACCUM_DATA status bit.

If a channel is inactive, a non–zero slew value should be written into CHx_CODE_SLEW before the channel is released. This write will be acted on immediately the reset is released.

If a TIC occurs during or soon after a slew the channel will

not be locked to the satellite, so the Measurement Data for that channel will not be of use.

The ability to read the Slew counter is included only for testing hardware or software and has no other use. It will only give a non–zero result if the read occurs during the actual slew operation. An example of a slewing event is shown in Fig.23.

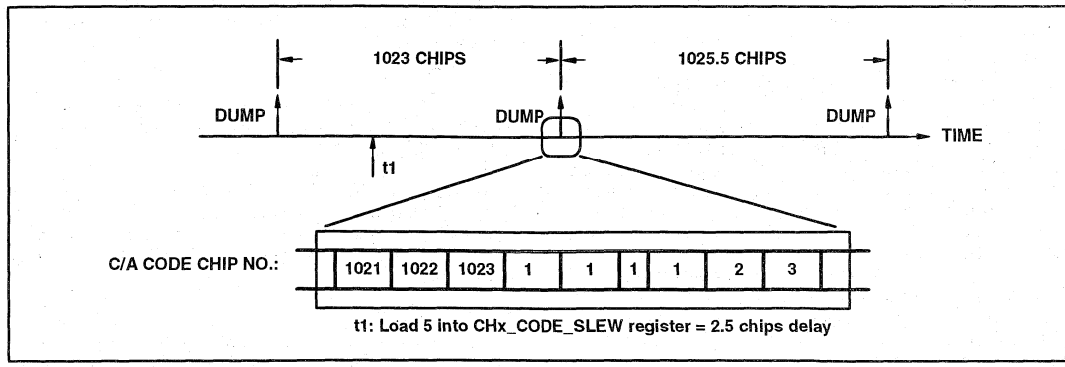


Fig. 23 : Slew timing in UPDATE mode

CHx_EPOCH_CHECK
(Read Address)

Bits 15 to 14: Not used.
Bits 13 to 8 : Instantaneous value of CHx_20MS_EPOCH.
Bits 7 to 5 : Not used.
Bits 4 to 0 : Instantaneous value of CHx_1MS_EPOCH.

Reading this address gives the instantaneous value of the CHx_1MS_EPOCH and the CHx_20MS_EPOCH counters. It can be used to verify if the Epoch counters have been properly initialised by the software. Its value is not latched and is incremented on each DUMP. To ensure the correct result, this register should be read only when there is no possibility of getting a DUMP during the read cycle, by synchronising the read to NEW_ACCUM_DATA. The ranges of these values are the same as those seen in the CHx_EPOCH register.

CHx_EPOCH
(Read Address)

Bits 15, 14, 7, 6 and 5: Not used. Read gives Low.
Bits 13 to 8: CHx_20MS_EPOCH: The 20 ms epoch counter value that was sampled at the last TIC event, with a valid range from 0 to 49.
Bits 4 to 0: CHx_1MS_EPOCH: The 1 ms epoch counter value that was sampled at the last TIC event, with a valid range from 0 to 19.

CHx_EPOCH_COUNT_LOAD
MULTI_EPOCH_COUNT_LOAD
ALL_EPOCH_COUNT_LOAD
(Write Address)

Bits 15, 14, 7, 6, and 5: Not used.
Bits 13 to 8: CHx_20MS_EPOCH: The value to be loaded into the 20 millisecond epoch counter, with a valid range from 0 to 49.
Bits 4 to 0: CHx_1MS_EPOCH: The value to be loaded into the 1 millisecond epoch counter, with a valid range from 0 to 19.

This operation is affected by the current channel mode, (PRESET or UPDATE). In UPDATE mode, the data written into these registers is immediately transferred to the 1 ms and 20 ms epoch counters. In PRESET mode however, the data is transferred only after the next TIC. It is important to load the CHx_EPOCH register last in the PRESET mode loading sequence because the trailing edge of a write to this register enables the whole PRESET operation on the next TIC. Refer to Detailed Operation of the GP2021 for more details of the PRESET mode. *

* Refer to page 23

CHx_I_TRACK,
CHx_Q_TRACK,
CHx_I_PROMPT,
CHx_Q_PROMPT
(Read Address)

Bits 15 to 0: Accumulated Data registers, which are used on each DUMP to store the 16–bit Integrate–and–Dump accumulator results. The values contained in the registers are 2's complement values with the valid range of the data from -2^{15} to $+(2^{15}-1)$.

These registers are read–only registers which can be read at any time. Their content is not protected by any overwrite protection mechanism, so the set of four registers must be read soon after a ACCUM_INT to be sure that newer data will not cause an overwrite part way through the set. The CHx_I_PROMPT and CHx_Q_PROMPT contain the Accumulated Data from the Prompt arm. The CHx_I_TRACK and CHx_Q_TRACK contain the Accumulated Data from the Tracking arm.

To track satellites correctly, only data read with the CHx_NEW_ACCUM_DATA bit set High should be used.

An overflow or underflow condition cannot be reached.

CHx_SATCNTL,
MULTI_ SATCNTL,
ALL_SATCNTL
(Write Address)

Bit	Bit Name
15	GPS_NGLON
14 to 13	TRACK_SEL
12	PRESET/UPDATEB
11	CODE_OFF/ONB
10	SOURCESEL
9 to 0	G2_LOAD (9 to 0)

CHx_SATCNTL is a write–only register that can be written into at any time. Any modification to the content is effective at the next DUMP in UPDATE mode or at the next TIC in PRESET mode for all bits, apart from PRESET/UPDATEB,

which defines whether a channel is in PRESET or UPDATE mode. It is important to program this register first when starting the initialisation of a PRESET sequence to get the channel into PRESET mode, or the other write operations will act too soon.

G2_LOAD (9 to 0), bits 9 to 0: C/A CODE SELECTION FUNCTION: The CHx_SATCNTL register programs the CODE GENERATOR by setting the G2 register to the appropriate starting pattern to generate the required GPS or INMARSAT–GIC codes. The G2_LOAD register may be programmed at any time but the value is only used when the code sequence restarts, at the following DUMP in UPDATE mode, or at the following TIC in PRESET mode. The pattern to load is the register state for the time of the second code chip. The following table shows the values required to select one of the 37 GPS or the 8 INMARSAT–GIC possible PRN (Pseudo Random Noise) patterns.

In UPDATE mode, the C/A code generated by the CODE GENERATOR will be changed at the DUMP following the write to CHx_SATCNTL and at this DUMP the Accumulated Data will be valid for the previous code selection. Later DUMPs will be valid for the new code.

If all zeros are loaded into the G2 register it will not clock out, and the G1 generator code will be seen on the output. This is an illegal state which is only of use for chip testing.

GPS PRN Signal No	BIT SETTING 9 to 0	GPS PRN Signal No	BIT SETTING 9 to 0
1	3F6H	24	338H
2	3ECH	25	270H
3	3D8H	26	0E0H
4	3B0H	27	1C0H
5	04BH	28	380H
6	096H	29	22BH
7	2CBH	30	056H
8	196H	31	0ACH
9	32CH	32	158H
10	3BAH	33	2B0H
11	374H	34*	058H
12	1D0H	35	18BH
13	3A0H	36	316H
14	340H	37*	058H
15	280H	201 GIC	2C4H
16	100H	202 GIC	10AH
17	113H	205 GIC	3E3H
18	226H	206 GIC	0F8H
19	04CH	207 GIC	25FH
20	098H	208 GIC	1E7H
21	130H	209 GIC	2B5H
22	260H	211 GIC	10EH
23	267H		

Table 9 : G2 LOAD settings required for satellite selection.

*C/A Codes 34 and 37 are equivalent.

Notes: PRN sequences 33 to 37 are reserved for non–satellite uses (e.g. ground transmitters).

PRN sequences 201 to 211 are selected for INMARSAT GIC (GPS Integrity Channel) use.

Due to the initialisation of the Early–Prompt–Late shift register, all codes will always start with a "1" for the first bit of the sequence after a Code change or a Code Slew. Subsequent cycles of the PRN sequence will be correct for the chosen satellite.

SOURCESEL, bit 10: Selects which input source to be used by the channel when in Real_Input mode. Low selects SIGN0 and MAG0, High selects SIGN1 and MAG1.

CODE_OFF/ONB, bit 11: When Low, the code is output normally, but when High, the Prompt, Early and Late codes are held High (code mixer outputs exactly follow inputs) and the Early–minus–late code is held LOW. This is intended for test purposes only.

PRESET/UPDATEB, bit 12: When High sets the channel into Preset mode, or when Low, sets the channel into Update mode. This bit is cleared to Low after the Preset function has been done, that is after the first TIC following the loading of the Epoch counters.

TRACK_SEL (1 and 0), bits 14 and 13: Select the appropriate code to be produced by the Tracking arm output of the code generator as follows:

14	13	CODE SELECT
0	0	Early code
0	1	Late code
1	0	Dithering code (alternating early and late)
1	1	Early–minus–late code

Table 10 : TRACK_SEL bit settings for Tracking arm code selection

When the dithering code has been selected, the Tracking arm will use the EARLY code for 20 periods of the Gold code, the LATE code for the next 20 periods and then this process of alternating between Early and Late code will be repeated indefinitely. The Tracking Arm will toggle between Early or Late Codes on every increment of a 20ms Epoch Count. Its state can be determined by reading the ACCUM_STATUS_C register.

The output code is a sequence of +1's and –1's for all code types except EARLY–MINUS–LATE where the result can also be a 0. In EARLY–MINUS–LATE mode the values are not the +2,0, –2 that results from the calculation (+1 or –1) –(+1 or –1), but are halved to +1, 0, –1. This must be considered when choosing thresholds in the software as the correlation results will be exactly half of the values otherwise expected.

GPS/NGLON, bit 15: Setting this bit to Low changes the C/A code generator mode to GLONASS mode, to generate the fixed 511 bit sequence used by all GLONASS Satellites. After a master reset, GPS mode is selected, but with all zeros in the G2 generator, the G1 code is seen at the output of the C/A code generator.

MEAS_STATUS_A

(Read Address)

Bit	Bit Name
15 to 14	Not Used
13	TIC
12	MEAS_INT
11	CH11_MISSED_MEAS_DATA
10	CH10_MISSED_MEAS_DATA
9	CH9_MISSED_MEAS_DATA
8	CH8_MISSED_MEAS_DATA
7	CH7_MISSED_MEAS_DATA
6	CH6_MISSED_MEAS_DATA
5	CH5_MISSED_MEAS_DATA
4	CH4_MISSED_MEAS_DATA
3	CH3_MISSED_MEAS_DATA
2	CH2_MISSED_MEAS_DATA
1	CH1_MISSED_MEAS_DATA
0	CH0_MISSED_MEAS_DATA

When a CHx_MISSED_MEAS_DATA status bit is High, it indicates that one or more sets of measurement data have been missed since the last read from this register. It is set High by a read from the Code Phase Counter of the same channel, when the previous value in the Code Phase Counter has not been read, and is reset by a read from the MEAS_STATUS_A register or by disabling the channel.

If this register is always read after the Code Phase Counter, it indicates whether measurement data has been missed before the last read of the Code Phase Counter. All CHx_MISSED_MEAS_DATA bits are set Low by a hardware or software reset.

The MEAS_INT bit is set High at each TIC and 50 ms before each TIC (if TIC period is greater then 50 ms), and is cleared by reading this register. The purpose of the bit, is a flag to the microprocessor, to time software module swapping. This bit is reset by a hardware master reset (RESETB at Low) but not by a software reset.

The TIC bit is set High at every TIC and is cleared by reading this register. The purpose of the bit is to tell the microprocessor that new Measurement Data is available. This bit is reset by a hardware master reset (RESETB at Low) but not by an MRB in RESET_CONTROL.

MULTI_CHANNEL_SELECT

(Write Address)

Bit	Bit Name
15 to 12	Not Used
11	CH11_SELECT
10	CH10_SELECT
9	CH9_SELECT
8	CH8_SELECT
7	CH7_SELECT
6	CH6_SELECT
5	CH5_SELECT
4	CH4_SELECT
3	CH3_SELECT
2	CH2_SELECT
1	CH1_SELECT
0	CH0_SELECT

CHx_SELECT, when set High, enables the Multi–channel write operations on CHx. This may be used to set several channels to mostly the same conditions. For a parallel search for one satellite, operations such as setting each Carrier DCO to the same frequency; or during that search, to adjust all selected channels by the same value, (such as a Code Slew to shift the code phases together to a new search area) could use this feature.

All CHx_SELECT are set Low by a (hardware or software) master reset.

PROG_ACCUM_INT

(Write Address)

Bits 15 to 13: Not Used.

Bits 12 to 0: ACCUM_INT Division Ratio.

The PROG_ACCUM_INT register location operates in conjunction with the INTERRUPT_PERIOD bit of the SYSTEM_SETUP register to set the period of the ACCUM_INT output. ACCUM_INT is generated by a 13 bit binary down counter which counts down to zero, producing an ACCUM_INT output. It then loads to a preset value stored in its preset register and starts to count down again. If the preset value is P, the count sequence is P, P–1, P–2, ..., 1, 0, P, P–1. Hence, the counter divides by P+1, producing an output with a period of (P+1) * clock period. Since the ACCUM_INT counter is clocked by the multi–phase clock, the clock rate is either 7 * clock period (nominally 40MHz, i.e. 25ns) for Real_Input mode, or 6 * clock period (nominally 35MHz, i.e. 28.571429ns) for Complex_Input mode. The value stored in the preset register can be modified in one of two ways: Either by toggling the INTERRUPT_PERIOD or FRONT_END_MODE bits of the SYSTEM_SETUP register, or by writing to the PROG_ACCUM_INT location. Either of these actions will overwrite the previous contents of the preset value and either one or both methods may be used. If the Interrupt Counter detects an edge on either the INTERRUPT_PERIOD or FRONT_END_MODE bits it will load one of four values in to the preset register, depending upon the new value of both INTERRUPT_PERIOD and FRONT_END_MODE. These four presets are as shown in Table 12.

The value for INTERRUPT_PERIOD = Low and FRONT_END_MODE = Low is also that loaded on a Master Reset. Alternatively the ACCUM_INT counter may be loaded by writing direct to the PROG_ACCUM_INT location. In this case the new ACCUM_INT period is as follows:

ACCUM_INT Period = (PROG_ACCUM_INT + 1) * 7/(40MHZ) (Real Input mode)

ACCUM_INT Period = (PROG_ACCUM_INT + 1) * 6/(35MHz) (Complex Input mode)

FRONT_END_MODE (In SYSTEM_SETUP)	INTERRUPT_PERIOD (In SYSTEM_SETUP)	Preset	ACCUM_INT Period
Low (Real_Input mode)	Low	0x0B45	(2885+1) * (7/40MHz) = 505.05000µs
Low (Real_Input mode)	High	0x1313	(4883+1) * (7/40MHz) = 854.70000µs
High (Complex_Input mode)	Low	0x0B81	(2945+1) * (6/35MHz) = 505.02857µs
High (Complex_Input mode)	High	0x1379	(4985+1) * (6/35MHz) = 854.74286µs

Table 12 : ACCUM_INT Period settings

PROG_TIC_HIGH, PROG_TIC_LOW

(Write Address)

PROG_TIC_HIGH Bits 4 to 0: More significant 5 bits of the TIC counter division ratio when programmed before a PROG_TIC_LOW.

PROG_TIC_LOW Bits 15 to 0: Least significant 16 bits of the TIC counter division ratio.

The PROG_TIC_HIGH and PROG_TIC_LOW register locations operate in conjunction with the FRONT_END_MODE bit of the SYSTEM_SETUP register to set the period of TIC. TIC is generated by a 21 bit binary down counter when it reaches zero. It then loads to a preset value stored in its preset register and starts to count down again. If the preset value is P, the count sequence is P, P–1, P–2, ..., 1, 0, P, P–1. Hence, the counter divides by P+1 producing an output with a period of (P+1) * clock period. Since the TIC counter is clocked by the multi–phase clock, the clock period is either 7 * clock period (nominally 40MHz i.e. 25ns) for Real_Input mode or 6 * clock period (nominally 35MHz i.e. 28.571429ns) for Complex_Input mode. The value stored in the preset register can be modified in one of two ways: Either by toggling the FRONT_END_MODE bit of the SYSTEM_SETUP register, switching into Complex_Input mode, or by writing to the PROG_TIC_HIGH/_LOW locations. Either of these actions will overwrite the previous contents of the preset value. If the TIC Counter detects an edge on the FRONT_END_MODE bit it will load one of two values into the preset register, depending upon its new value. These two presets are as shown in Table 13.

The value for FRONT_END_MODE = Low is also that loaded on a Master Reset. Alternatively, the TIC counter may be loaded by writing directly to the PROG_TIC locations. This may be achieved in one of two ways: Either the PROG_TIC_HIGH value can be written, followed by the PROG_TIC_LOW value, (at which point the full 21 bits are transferred to the preset register), or just the PROG_TIC_LOW value may be written to modify the lower 16 bits of the preset value. It should be noted that in the former case, the top 5 bits programmed as PROG_TIC_HIGH are stored locally to the TIC counter and even if a write to PROG_TIC_LOW does not directly follow the write to PROG_TIC_HIGH, the next PROG_TIC_LOW write will still transfer all 21 bits. It is also necessary to ensure that the write to PROG_TIC_HIGH precedes the write to PROG_TIC_LOW, rather than follows it. One further point to note is that the transfer of data to the TIC counter data latches occurs under control of the multi–phase clock write cycle and the write to the preset register happens subsequent to the main internal write. To ensure correct operation, a write to SYSTEM_SETUP, toggling the FRONT_END_MODE bit should not be directly preceded or followed by a write to PROG_TIC_LOW. In addition to the 300ns delay normally required between write cycles, a further 100ns delay is required between these two types of writes. A write to SYSTEM_SETUP toggling the FRONT_END_MODE bit followed directly by a PROG_TIC_HIGH / PROG_TIC_LOW sequence is permissible, since the write to PROG_TIC_HIGH does not instigate a change of the preset register contents within the TIC counter.

Using the PROG_TIC write locations the TIC period is as follows:

TIC Period (Real_Input) = ((PROG_TIC_HIGH * 65536) + PROG_TIC_LOW+1) * 7/(40MHZ)

TIC Period (Complex_Input) = ((PROG_TIC_HIGH * 65536) + PROG_TIC_LOW+1) * 6/(35MHZ)

FRONT_END_MODE (In SYSTEM_SETUP)	Preset Loaded	TIC Period
Low (Real_Input mode)	0x08B823	(571427+1) * 7/(40MHz) = 99.999900ms
High (Complex_Input mode)	0x08E6A4	(583332+1) * 6/(35MHz) = 99.999943ms

Table 13 : TIC period setting

RESET_CONTROL

(Write Address)

Bit	Bit Name
15	Not used.
14	Not used.
13	Not used.
12	CH11_RSTB
11	CH10_RSTB
10	CH9_RSTB
9	CH8_RSTB
8	CH7_RSTB
7	CH6_RSTB
6	CH5_RSTB
5	CH4_RSTB
4	CH3_RSTB
3	CH2_RSTB
2	CH1_RSTB
1	CH0_RSTB
0	MRB, Active LOW software master reset

MRB: When Low (a software reset), the effect is similar to a hardware reset except that the clock generator, the time base generators, measurement data and peripheral functions are not affected and the Status bits ACCUM_INT, DISCIP, DISCIP_GLITCH, MEAS_INT, and TIC are not reset. MRB should be set to High to allow access to all of the various registers. MRB is set High by a hardware reset.

CHx_RSTB: When set active Low, the reset bit inhibits propagation of the clock phases to the CHx tracking channel and resets the Accumulated Data flags, Code DCO and Carrier DCO accumulators, the I & D accumulators, and the Code Phase Counter. A CHx_RSTB does not reset the Carrier Cycle, Code Slew or the Epoch counters. At the end of the reset, the channel enable resets the code generator to a previously programmed start phase. This is all required for the parallel search algorithm of one satellite signal using many channels in order to start from a known relative code phase on all the channels. All of the control registers in CHx can be programmed and read as usual during the reset state. To restart normal operation in several different channels at the same time, the corresponding CHx_RSTB bits should be set to High during the same write operation. All CHx_RSTB are set Low by a master reset, (both hardware and software), so a write Low to bit 0 of this register will force a Low onto bits 12 to 1 irrespective of what was on the bus.

Power consumption can be kept to a minimum by setting CHx_RSTB Low when a channel is not required.

STATUS
(Write Address)

Bits 15 to 0: not used

A write operation to this location, irrespective of the data on the bus, latches the state of all status bits contained in ACCUM_STATUS_A, ACCUM_STATUS_B, and ACCUM_STATUS_C registers. Performing a write to STATUS prior to reading the status registers ensures reading of stable status values. The latch takes effect within 300 ns of the trailing edge of the write pulse. The active edge transition of the ACCUM_INT signal will also latch the state of the status bits, thus it is not necessary to write to STATUS when the status registers are to be read as a response to the ACCUM_INT signal in an interrupt handling routine. The write to STATUS is required only when the status registers are read at times that are not synchronised to the interrupts. These two mechanisms are mutually exclusive and should not be used together – if both are used, a write to STATUS soon after the occurrence of an ACCUM_INT signal can result in confused readings. To avoid conflict the INTERRUPT_ENABLE in the SYSTEM_SETUP register should be set to Low if writes to STATUS are to be used.

If the INTERRUPT_ENABLE bit in SYSTEM_SETUP register is set to Low, the interrupt will not latch the status bits in the status registers, but a STATUS write access will do so.

SYSTEM_SETUP
(Write Address)

Bit	Bit Name
15 to 11	Not used
10	MEAS_INT_SOURCE
9	OPS_DRIVE_SEL
8	IPS_3V_MODE
7	INTERRUPT_PERIOD
6	FRONT_END_MODE
5	INTERRUPT_ENABLE
4	DISCOP_SELECT_100KHZ
3	DISCOP_SELECT_TIMEMARK
2	DISCOP_SELECT_CH0_DUMP
1	DISCOP
0	CARRIER_MIX_DISABLE

MEAS_INT_SOURCE: When set High the MEAS_INT output is cleared by a read of MEAS_STATUS_A, when Low by a read of ACCUM_STATUS_B. A master reset forces the MEAS_INT_SOURCE bit Low.

OPS_DRIVE_SEL: When set High this control bit increases the size of the output driver on ACCUM_INT, MEAS_INT, and D(15:0) pins so as to increase the drive of these pins if they are driving a large load. Master reset forces OPS_DRIVE_SEL to Low.

IPS_3V_MODE: When set High this control bit sets the input buffers on SIGN0, MAG0, SIGN1, and MAG1 for signals centred on mid–supply, for use with a Front–end running from a 3V supply. When Low, sets the thresholds to TTL levels, for 5V operation. Master reset forces IPS_3V to Low.

INTERRUPT_PERIOD: When Low, the approximate interrupt period is set to 505µs and when High it is set to 854 µs. For more detail see the description of PROG_ACCUM_INT. Master reset forces INTERRUPT_PERIOD bit to Low.

FRONT_END_MODE: Selects either Real_Input mode when Low or Complex_Input mode when High. Master reset forces FRONT_END_MODE to Low.

INTERRUPT_ENABLE: When set Low the effect of the ACCUM_INT and MEAS_INT interrupts are disabled (masked) and when set High both are enabled. Master reset forces INTERRUPT_ENABLE to Low.

Bits 4 to 1 The signal provided on the DISCOP pin can be selected according to Table 14.

Bit				Signal On DISCOP output
4	3	2	1	
0	0	0	0	0 (Reset condition.)
0	0	0	1	1
0	1	0	X	Timemark
0	X	1	X	Ch0 DUMP
1	X	X	X	100kHz Square wave

Table 14 : DISCOP selection

CARRIER_MIX_DISABLE: When High the Carrier mixers are all driven by a fixed '+1' level on the Carrier DCO input port, so that the input data is passed unaltered to the Code mixer. Master reset forces the CARRIER_MIX_DISABLE bit to Low.

TEST_CONTROL
(Write Address)

Bit	Bit Name
15 to 12	Not Used
11 to 9	PATH_SEL<2:0>
8	EN_SCANPATH
7	Not Used
6	TEST_CACODES
5	TEST_DATA
4	TEST_SOURCE
3	TM_TEST
2	FE_TEST
1	EN_DUMMYTICS
0	EN_DUMMYDUMP

This register is purely to enable various test modes. A Master Reset will set all bits to Low, giving normal operation.

EN_DUMMYDUMP: When High, this bit changes the function of the NOPC/NINTELMOT input pin to be a DUMMYDUMP input, and if in Standard Interface Mode it also forces the microprocessor mode to Motorola. A DUMMYDUMP will operate in the same way as a normal DUMP (reset all of the code generators and transfer the contents of all integrators into the Accumulated Data registers). Each Low to High transition of NOPC/NINTELMOT will cause a DUMMYDUMP and if NOPC/NINTELMOT is already High when EN_DUMMYDUMP is set, one will also occur immediately. Selecting Dummy dump mode does not inhibit normal DUMP events. The NOPC/NINTELMOT pin must be held High for at least 200 ns for each DUMMYDUMP.

EN_DUMMYTICS: When High this bit changes the function of the DISCIP input pin to a DUMMYTIC input. This replaces the TIC from the timebase generator so that a TIC effect will only occur when there is a Low to High transition on DISCIP, to latch new Measurement Data. The DISCIP pin must be held High for at least 200 ns for each DUMMYTIC.

FE_TEST: When High this test control forces the SIGN input to channel 11 and the MAG input to channel 5 both to Low. This allows the evaluation of the front_end SIGN (on channel 5) and MAG (on channel 11) duty cycles. The Front–end to be tested is selected by the SOURCESEL bits in CH5_SATCNTL and CH11_SATCNTL.

To get the SIGN and MAG count correctly into the accumulators, both the carrier and code mixers must be made transparent.

The carrier mixing may be disabled by either: (1) Setting

CARRIER_MIX_DISABLE (bit 0 in SYSTEM_SETUP) to High to force a +1 on the Carrier DCO inputs to all channels or, (2) If continued position finding is required from the other channels during the test, by setting CH5_ and CH11_CARRIER_DCO_INCR to all 0's, to give a constant level (zero frequency). This level should be set to a known value by putting channels 5 and 11 briefly into the reset state (by using RESET_CONTROL register bits 6 and 12) during the time their Carrier DCO's are programmed to zero frequency. This reset forces the phase to all 0's and hence the drives to the Prompt In–phase mixer to a fixed +1 and not a randomly selected –2, –1, +1, or +2 that would result from just setting the frequency.

The C/A code mixing must be disabled by setting CODE_OFF/ONB (bits 11 in both CH5_ and CH11_SATCNTL) to High. However, as the period of the count is set by the DUMPs from the Code Generator, the DCO clock to the Code Generator must be set to the required frequency by programming the Code DCO even though the code output is disabled. A typical value is the frequency for the nominal code chipping rate, so that the SIGN and MAG counts are over a millisecond.

The results of monitoring the Front–end of the receiver may be used for fault diagnosis and also for tuning the parameters in the software for optimum satellite tracking with the particular Front–end or SIGN/MAG duty cycle.

To find the duty cycle of the SIGN signal, channel 5 is used. The In–phase accumulator CH5_I_PROMPT will add +1 for each SIGN sample at High and will add –1 for each SIGN sample at Low, so if the duty cycle is correct at 50%, the sum will always be close to zero and only differ by the imbalance of sampling at the beginning and end of the integration period. The duty cycle may be calculated as follows:

N = Total No of samples in integration period.
N_{SIGN1} = Total No of samples for which SIGN was High.
N_{SIGN0} = Total No of samples for which SIGN was Low.
ACC5 = Total value in the CH5_I_PROMPT accumulator, as read after a DUMP.

$N = N_{SIGN1} + N_{SIGN0}$,
$ACC5 = N_{SIGN1} - N_{SIGN0}$

SIGN duty cycle = $R_S = N_{SIGN1} / N = (N + ACC5) / 2N$ (nominally 0.50)

To find the duty cycle of the MAG signal, channel 11 is used. The In–phase accumulator CH11_I_PROMPT will add –3 for each MAG sample at High and will add –1 for each MAG sample at Low. If the duty cycle is correct (30%), the sum will be: –1.6 * (Number of samples) plus an allowance for the imbalance of sampling at the beginning and end of the integration period. The duty cycle may be calculated as follows:

N = Total No of samples in integration period.
N_{MAG3} = Total No of samples for which MAG was High
N_{MAG1} = Total number of samples for which MAG was Low
ACC11 = Total value in the CH11_I_PROMPT accumulator, as read after a DUMP.

$N = N_{MAG3} + N_{MAG1}$,
$ACC11 = -3 * N_{MAG3} - N_{MAG1}$

MAG duty cycle, $Rm = Nmag3 / N = -(N + ACC11) / 2N$ (nominally 0·30).

TM_TEST: When High this bit puts all the Tracking Modules into a test mode, where it is possible to write to all CHx_CARRIER_CYCLE_COUNTERs and all CHx_CODE_PHASE_COUNTERs.

TEST_SOURCE: When High this bit enables a self–test generator formed from the CH0 Code Generator. The data replaces the SIGN0 and MAG0 inputs. It has a chip rate and phase set by the CH0_CODE_DCO and a carrier frequency set by the CH0_CARRIER_DCO. The code is set by writing the appropriate start value into the CH0_SATCNTL register, and the CH0_SLEW_COUNTER can be programmed to delay the start of the code generation by a number of half code chips. The three most significant bits of the Carrier DCO are decoded to give the SIGN with 50% of Highs and the MAG with 25% of Highs. The sign of the data pattern is set by TEST_DATA, EXORed with the CH0 C/A code.

TEST_DATA: This bit sets the sign of the modulation of the test data generated when TEST_SOURCE is set.

TEST_CACODES: When High, the inverted PROMPT codes for all channels, 0 to 11, are available for output on data bus bits 0 to 11 and can be seen in parallel by a read to any CH6 to CH11 read address.

EN_SCANPATH: When High the chip is in scan test mode, whereby:

DISCIP 1	becomes	SCAN_IN
DISCOP	becomes	SCAN_OUT
MULTI_FN_IO	becomes	SCANCLK
NOPC/NINTELMOT	becomes	SCANSEL

It should be noted that the DISCOP = SCAN_OUT function may be over–ridden by the DISCOP_SELECT_100KHZ function of SYSTEM_SETUP. It should also be noted that for correct operation the MULTI_FN_IO pin should be configured as a Discrete or Scan Clock Input via the IO_CONFIG register.

PATH_SEL<2:0>: To allow for simple factory testing of the chip, the GP2021 contains six separate scan paths, one for each of the major counters in the chip. Only one of these paths may be enabled at any time and the scan path to be used is selected via the PATH_SEL<2:0> bits as follows:

PATH_SEL<2:0>	Scan Path Selected
000	RTC Counters
001	ACCUM_INT Counter
010	TIC Counter
011	100KHz Output Counter
100	Timemark Pulse Width Counter
101	PLL_LOCK Filter Counter
11X	Not Used

TIMEMARK_CONTROL (Write Address)

Bit	Bit name
15 to 7	not used
6 to 2	FREE_RUN_RATIO
1	FREE_RUN_TIMEMARK
0	ARM_TIMEMARK

The TIMEMARK Generator operates in one of two ways, either in armed mode, (not related to ARM System Mode) or in free run mode. In armed mode setting the ARM_TIMEMARK bit arms the TIMEMARK generator which subsequently produces a TIMEMARK output pulse coincident with the next rising edge of TIC. This then resets the ARM_TIMEMARK bit ready for a new arming sequence in the future. Alternatively, the TIMEMARK generator can be used in free–run mode, by

setting the FREE_RUN_TIMEMARK bit High. This disables the ARM_TIMEMARK bit. In free run mode a TIMEMARK pulse is produced coincident with the first rising edge of TIC after the FREE_RUN_TIMEMARK bit has been set, and then on an integer number of TIC's determined by the FREE_RUN_RATIO bits. In free run mode the TIMEMARK period is:

TIMEMARK Period = (FREE_RUN_RATIO + 1) * TIC Period (Free run mode)

All the bits of TIMEMARK_CONTROL are cleared to Low by a Master Reset.

X_DCO_INCR_HIGH
(Write Address)

This register may be used to write the high bits for any Carrier or Code DCO in any channel. A write to X_DCO_INCR_HIGH must always be followed by a write to the appropriate CHx_CARRIER_DCO_INCR_LOW or CHx_CODE_DCO_INCR_LOW to define the destination and to complete the action.

Using X_DCO_INCR_HIGH rather than CHx_CARRIER_DCO_INCR_HIGH gives a quicker way of loading the whole DCO's values because the _LOW write may follow the X_DCO_INCR HIGH write immediately (without incurring a 300ns wait).

PERIPHERAL FUNCTIONS REGISTERS

The addresses for the Peripheral Functions Registers are shown in the GP2021 Register Map.

These registers may be either 8 or 16 bits wide. Registers which are byte wide are accessed via the top 8 bits of the data bus, D<15:8>. During a byte wide read D<7:0> are held Low.

Each of the registers for the Real Time Clock, Dual UART, System and General Control functions are described below.

Real Time Clock and Watchdog

The registers in the Real Time Clock are all byte wide.

RTC_LS,
RTC_2ND,
RTC_MS ,
(Read Addresses)

The clock time is output in these three eight bit read only registers. All three registers are latched when a read is performed of the LS Byte Register, so this should be read first.

In Power Down Mode the clock continues to run but access to these registers is not possible.

CLOCK RESET
(Write Address)

A write to this address resets the clock divider and counter, regardless of the data word written.

WATCHDOG RESET
(Write Address)

A write to this address resets the watchdog timer, regardless of the data word written.

DUART

All the registers within the DUART are byte wide.

CONFIG_A, CONFIG_B (Write Address)

These registers allow the UARTs to be configured for receive baud rate, parity and loopback. The configuration bit functions are shown in Table 15. The missing binary combinations of bit settings should not be used as the results would be indeterminate.

Note that all bits are set Low by a UART A/B or a System reset, thus causing UART A/B to default to a receive baud rate of 300, no parity and no loopback.

Bit Settings					Function
Bit	11	10	9	8	Receiver Baud Rate
	0	0	0	0	300
	0	0	0	1	600
	0	0	1	0	1200
	0	0	1	1	2400
	0	1	0	0	4800
	0	1	0	1	9600
	0	1	1	0	19.2k
	0	1	1	1	38.4k
	1	0	0	0	76.8k
Bit	13	12			Parity
	0	0			No parity–bit not set or checked for.
	1	1			Odd parity–parity added so that the total number of '1's in the word is odd.
	1	0			Even parity–parity added so that the total number of '1's in the word is even.
Bit	14				Loopback
	0				No loopback–normal operation
	1				Loopback–the Tx output drives the Rx input and the Tx pin is held HIGH.
Bit	15				Test mode
	0				Test mode bit in Ch A only used for chip testing only. This bit must be set Low for Normal operation.
	1				Test mode

Table 15 : Configuration of UARTs through CONFIG_A and CONFIG_B registers.

STATUS_A, STATUS_B (Read Address)

Reading from these register addresses will give the current value of the channels status bits. The Status bit functions are as shown in Table 16.

Bit	SET (High) by	CLEARED (Low) by	RESET to
8	RX Valid Data Available	No RX Data	Low
9	RX FIFO Full	RX FIFO Not Full	Low
10	RX FIFO Overflow	Read of UART Status Register	Low
11	TX Transmitting	TX Register Empty	Low
12	TX FIFO Full	TX FIFO Not Full	Low
13	Parity Error Occurred	Read of UART Status Register	Low
14	Framing Error Occurred	Read of UART Status Register	Low
15	Not Used (Held High)		

Table 16 : Status bits available when reading the STATUS_A and STATUS_B registers.

RESET_A, RESET_B (Write Address)

Writing to this register will reset the UART A/B, regardless of the data word written.

TX_DATA_A, TX_DATA_B, RX_DATA_A, RX_DATA_B (Write / Read Address)

These are Read/Write addresses to UARTs A and B, which allow bytes to be written to the TX FIFOs or received from the RX FIFOs.

TX_RATE_A, TX_RATE_B (Write Address)

These are write registers for UARTs A and B which allow the Transmit baud rates to be set as shown in Table 17. The missing binary combinations of bit settings should not be used as the results would be indeterminate.

Bit	11	10	9	8	Transmit Baud Rate
	0	0	0	0	300
	0	0	0	1	600
	0	0	1	0	1200
	0	0	1	1	2400
	0	1	0	0	4800
	0	1	0	1	9600
	0	1	1	0	19.2k
	0	1	1	1	38.4k
	1	0	0	0	76.8k

Table 17: Transmit baud rate settings in the TX_RATE_A and TX_RATE_B registers.

Bits 12 to 15 are not used and may be set High or Low. Note that bits 8 to 11 are set Low by a UART A/B or System reset, thus causing the Transmitter to default to a baud rate of 300.

System Control

WAIT_STATE (Write / Read Address)

This is a Read/Write register (8 bits wide), which allows the ROM (Read/Write) wait state and EEPROM and Spare (Read) wait states to be configured via bits 8 to 11. EEPROM and SPARE read accesses consist of 2–5 wait states whilst MCLK is High, increasing the read access time, followed by 1 trailing wait state whilst MCLK is Low to allow for a greater bus release time. The Chip revision number appears on bits 12 to 15 when read.

Bit	9 8	ROM (Read/Write) Wait States
	0 0	1
	0 1	2
	1 0	3[1]
	1 1	Unused (3)
Bit	**11 10**	**EEPROM and Spare (Read) Wait States**
	0 0	2+1
	0 1	3+1
	1 0	4+1
	1 1	5+1 [1]

Table 18 : WAIT_STATE register settings.

Note [1]. The conditions after a reset are:–
ROM wait states= 3, EEPROM and Spare wait states = 5+1.

SYSTEM_CONFIG (Write / Read Address)

This is a Read/Write register (8 bits wide), which allows the Watchdog Function to be enabled and disabled via bit 9. Note that following a System reset this bit is set Low, thus enabling the watchdog.

Bit	9	Watchdog Function
	0	Enabled
	1	Disabled

Table 19 : Enabling the Watchdog function through the SYSTEM_CONFIG register.

Bits 15 to 10 and 8 are not used and could be set High or Low. The Chip revision number appears on bits 12 to 15 when read.

SYSTEM_ERROR_STATUS

This is an 8 bit wide Read only register, and allows the source of a system reset to be determined via bits 11 to 8. It is reset to all Low after being read. The Chip revision number appears on bits 12 to 15 when read.

Bit 8 : Set during a system reset , when the source of the reset is a PLL_LOCK failure.
Bit 9 : Set during a system reset, when the source of the reset is the Watchdog.
Bit 10 : Set during a system reset, when the source of the reset is a POWER_GOOD failure.
Bit 11 : Set during a system reset, when the source of the reset is the external NRESET_IP. Note that this reset source is only available in Standard Interface Mode.

CHIP_REVISION (Read Addresses)

The CHIP_REVISION register is a read only register which exists as the high 4 data bits of the Wait State, System Configuration and System Error Status registers. A read of any of these three registers will output the CHIP_REVISION information on bits 15 to 12. This register is intended to allow software discrimination of revisions of the GP2021, both pre–production revisions and possible customer specific variants. The initial production version of the GP2021 will have a CHIP_REVISION of 0011.

DATA_RETENT
(Write / Read Address)

This is a byte wide Read/Write register which can be used to store a predetermined value, which can be interrogated in order to determine whether a total power loss (below the data retention level) has occurred.

General Control

IO_CONFIG
(Write / Read Address)

The IO_CONFIG register is a full 16 bit wide read/write register containing two separate elements: A 16 bit wide read location which allows the controlling microprocessor to view the input level on all the Discrete and Multi Function inputs, and a 16 bit wide write location for configuration of the Discrete and Multi Function I/O pins.

IO_CONFIG Read: A read of the IO_CONFIG address will latch the logic level of a number of input pins and output these levels to the microprocessor via the 16 bit data bus. This allows the microprocessor to read the input levels on all the Discrete and Multi Function Inputs from a single location. The bit allocations are as follows:

Bit	Input Pin
15	RXB
14	RXA
13	DISCOP
12	DISCIP
11	MAG1
10	SIGN1
9	MAG0
8	SIGN0
7	MULTI_FN_IO
6	NBRAM
5	DISCIO
4	NARMSYS
3	NBW/WRPROG
2	NMREQ
1	NOPC/NINTELMOT
0	NRW

It should be noted that the usefulness of a number of these inputs as Discrete Inputs for System Control is dependant upon the Interface Mode of the GP2021. For instance it is possible to use the NOPC/NINTELMOT pin as a Discrete Input in ARM System mode if the DEBUG function is disabled, whereas this pin could not be used as a Discrete Input in Standard Interface Mode. Similarly, NMREQ could be used as a Discrete Input in Standard Interface Mode but not in ARM System Mode.

IO_CONFIG Write: The IO_CONFIG write location allows the configuration of the multi purpose I/O pins DISCIO and MULTI_FN_IO. The register bit assignments are as follows:

Bit	Bit Name
15 to 13	Not Used
12	MULTI_FN_IO_SELECT_TIMEMARK
11	MULTI_FN_IO_SELECT_100KHZ
10	MULTI_FN_IO_LEVEL
9 to 8	MULTI_FN_IO_CONFIG
7 to 4	Not Used
3	DISCIO_SELECT_TIMEMARK
2	DISCIO_SELECT_100KHZ
1	DISCIO_LEVEL
0	DISCIO_CONFIG

DISCIO_CONFIG: When set High this bit configures the DISCIO pin as a Discrete Output, when low the DISCIO pin is configured as a Discrete Input. A Master Reset sets the DISCIO_CONFIG bit Low.

DISCIO_SELECT TIMEMARK,
DISCIO_SELECT_100KHZ,
DISCIO_LEVEL:

When configured as an output, the DISCIO pin can be setup to give a signal as determined by Table 20.

Bit			DISCIO output value
3	2	1	
0	0	0	0
0	0	1	1
0	1	X	100kHz square wave
1	X	X	TIMEMARK

Table 20 : DISCIO output selection.

At power on reset, the DISCIO output value = 0 setting is chosen. The 100kHz square wave is derived from the Master Clock and is useful for measuring its drift.

MULTI_FN_IO_SELECT TIMEMARK,
MULTI_FN_IO_SELECT_100KHz,
MULTI_FN_IO_LEVEL:

When configured as an output, the MULTI_FN_IO pin can be setup to give a signal as shown in Table 21

Bit			MULTI_FN_IO value
12	11	10	
0	0	0	0
0	0	1	1
0	1	X	100kHz square wave
1	X	X	TIMEMARK

Table 21 : MULTI_FN_IO output selection.

MULTI_FN_IO_CONFIG: These 2 bits configure the function of the MULTI_FN_IO input as follows:

Bits <9:8>	MULTI_FN_IO Function
00	Digital System Test Enable Input
01	TRIGGER Input
10	Discrete Input (See Description) / Scan Clocks Input
11	Discrete Output

Master Reset sets bits 9 and 8 to Low.

MULTI_FN_IO as Digital System Test Enable Input: Allows testing of the Digital Section of the System Board. In this mode, when MULTI_FN_IO is High, the RXA pin replaces the Differential Master Clock Inputs and the RXB pin acts as an RTC Reset input. The PLL_LOCK Filter is also disabled. For more information see the Digital System Test Mode description.

MULTI_FN_IO as TRIGGER Input: The DEBUG function is enabled if in ARM System mode and the MULTI_FN_IO pin acts as the TRIGGER input to the DEBUG block. For more information see the DEBUG Block Description.

MULTI_FN_IO as Discrete Input / Scan Clocks: In this mode the pin has 2 functions: As a discrete input and as the Scan Clocks Input for chip scan path testing. It should be noted that the MULTI_FN_IO pin should only be used as a discrete input with caution. Since the Master Reset default is for MULTI_FN_IO to act as the Digital System Test Enable input it must be guaranteed that anything driving this pin as a discrete input must have a Low output until the IO_CONFIG register can be written to and Discrete Input Mode enabled.

TEST_CONFIG (Write Address)

The TEST_CONFIG register is a 3 bit wide write–only register which complements the TEST_CONTROL register of the Correlator but contains chip test control bits for Peripheral Functions. The register bit assignments are as follows:

Bit	Bit Name
10	RTC_TEST_COUNT
9	RTC_RESET_ENABLE
8	WDOG_RESET_DISABLE

RTC_TEST_COUNT : When set High this bit splits up the 24 bit counter of the RTC which counts seconds into a number of 4 bit counters to allow easier chip testing. The 24 bit RTC Counter is not Scan Path Testable. A Master Reset sets the RTC_TEST_COUNT bit Low.

RTC_RESET_ENABLE: When set High this bit enables the RXB pin to act as an RTC Reset input, which then resets the RTC and Watchdog counters whenever RXB is taken high. This function is intended for factory testing of the GP2021. A Master Reset forces the RTC_RESET_ENABLE bit Low.

WDOG_RESET_DISABLE: When set High this bit inhibits the production of System Resets from the Watchdog counter, without disabling the Watchdog Counter itself. This function is intended for Scan Path Testing of the Watchdog and RTC Counters. A Master Reset forces the WDOG_RESET_DISABLE bit Low.

DATA_BUS_TEST (Write / Read Address)

This is a 16 bit read/write register, whose function is to allow a simple test of the 16 bit wide data bus to be performed, by writing a 16 bit number and by checking that the same value can be read back.

ABSOLUTE MAXIMUM RATINGS

These are not the operating conditions, but are the absolute limits which if exceeded, even momentarily, may cause permanent damage.
To ensure sustained correct operation the device should be used within the limits given under Electrical Characteristics.
It is essential for both V_{DD} and V_{SS} to be present before input signals are applied.

Supply Voltage (V_{DD}) from ground (V_{SS}):	–0.3 to+6.0V
Input Voltage (any input pin):	V_{SS} –0.3V to V_{DD}+ 0.3V
Output Voltage (any output pin):	V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature:	–55°C to +150°C

Electrostatic Discharge Protection (ESD)

The device is able to withstand an electrostatic discharge level of 2kV from 100pF through 1500Ω between any two pins in either polarity (MIL. Std. 883 Human body model).

Crystal Specification

Frequency:	32.768kHz
Temperature range:	–40°C to +85°C
Series resistance:	50kΩ typ, 100kΩ max
Load capacitance:	10pF typical

ELECTRICAL CHARACTERISTICS

T_{amb}= −40°C to +85°C, V_{DD}= +5V ±10%. The input thresholds and output voltage limits for the logic signal pins are tested and guaranteed by production test. All other parameters are guaranteed by characterisation and design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Supply Current	I_{DD}		22		mA	0 Channels enabled.
			27		mA	4 Channels enabled.
			32		mA	8 Channels enabled.
			38		mA	12 Channels enabled.
			20	150	µA	Power Down Mode 2.2V – 3.3V (Note 3)
			50	500	µA	Power Down Mode 5.0V (Note 3)
Battery backup Voltage	V_{BATT}	2.2			V	Power Down Mode
All TTL Inputs, with and without Pull–up or Pull–down Resistors: type TTL						
High level Input Voltage		2.0			V	
Low level Input Voltage				0.8	V	
Schmitt Trigger inputs Type ST1						
Positive–going Threshold	VI +		1.9	2.3	V	V_{DD} = 3V
Negative–going Threshold	VI –	0.8	1.2		V	V_{DD} = 3V
Hysteresis	Vh	0.35	0.7		V	V_{DD} = 3V
Schmitt Trigger inputs Type ST2						
Positive–going Threshold	VI +		1.72	2.32	V	
Negative–going Threshold	VI –	0.72	1.10		V	
Hysteresis	Vh	0.3	0.62		V	
Master clocks : type Diff						Note 2
Input Voltage High		$0.8V_{DD}$			V	D.C. coupled
Input Voltage Low				$0.2V_{DD}$	V	D.C. coupled
OR						
D.C. coupled differential sinewave (pk–pk)		130			mV	Mid point at nominal 4.3V
OR						
Peak to Peak single sinewave		600			mV	AC coupled
Crystal Oscillator Type XTLI, XTLO						
Frequency Range	f_{osc}		32	1000	kHz	
Amplifier Transconductance	gm	220	550	2500	µA/V	
Output Impedance	Z0	20	56	100	kΩ	

ELECTRICAL CHARACTERISTICS(cont.)

T_{amb}= −40°C to +85°C, V_{DD}=+5V ±10%. The input thresholds and output voltage limits for the logic signal pins are tested and guaranteed by production test. All other parameters are guaranteed by characterisation and design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Power level 6 Outputs: types OP6 and OPT6						
Output Voltage High	V_{OH}	$0.8V_{DD}$			V	I_{OH} = −12mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 12mA
Output short circuit current	IOS		270 150		mA mA	V_{DD} = max VO = V_{DD} V_{DD} = max VO = 0V
Tri–state output leakage current	IOZ		<10		µA	VOH = GND or V_{DD}
Output capacitance	COUT		5		pF	
Power Level 3 Outputs : types OP3 and OPT3						
Output Voltage High	V_{OH}	$0.8V_{DD}$			V	I_{OH} = −6mA
Output voltage Low	V_{OL}			0.4	V	I_{OL} = 6mA
Output short circuit current	IOS		135 75		mA mA	V_{DD} = max VO = V_{DD} V_{DD} = max VO = 0V
Tri–state output leakage current	IOZ		<10		µA	VOH = GND or V_{DD}
Output capacitance	COUT		5		pF	
Power Level 2 Outputs: types OP2 and OPT2						
Output voltage High	V_{OH}	$0.8V_{DD}$			V	I_{OH} = −4mA
Output voltage Low	V_{OL}			0.4	V	I_{OL} = 4mA
Output short circuit current	IOS		90 50		mA mA	V_{DD} = max VO = V_{DD} V_{DD} = max VO = 0V
Tri–state output leakage current	IOZ		<10		µA	VOH = GND or V_{DD}
Output capacitance	COUT		5		pF	
Power Level 1 Outputs: types OP1 and OPT1						
Output Voltage High	V_{OH}	$0.8V_{DD}$			V	I_{OH} = −2mA
Output Voltage Low	V_{OL}			0.4	V	I_{OL} = 2mA
Output short circuit current	IOS		45 25		mA mA	V_{DD} = max VO = V_{DD} V_{DD} = max VO = 0V
Tri–state output leakage current	IOZ		<10		µA	VOH = GND or V_{DD}
Output capacitance	COUT		5		pF	

Note 1: Any unused inputs must be tied High or Low.
Note 2: The input pair CLK_T, CLK_I may be driven by CMOS logic levels (D.C. coupled) or A.C. coupled or by a low amplitude differential sinewave (D.C. coupled e.g. GP2010). If a single logic level is to be used this should drive CLK_T with the CLK_I pin biased to mid supply. If a single sinewave clock is to be used this should drive CLK_T through a capacitor, with both of the CLK_T/CLK_I pins biased to approximately two thirds supply. See Fig. 24 for a suggested circuit.
Note 3: These values apply when the 32kHz oscillator circuit is not running.
Note 4: The operation of the feature whereby input levels and output drive strengths can be modified is not guaranteed by the existing factory testing procedure.

PIN TYPES

The following Table defines the type of each pin and additional notes relating to them.

Pin No	Pin Name	Pin Type	Input Type	Pull Up/Dn	O/P Type	Tri-State	Notes
1	MULTI_FN_IO	I/O	ST2	75k dn	OPT3	YES	1
2	POWER_GOOD	IP	ST2	none	–	–	
3	NRESET_OP	OP	–	–	OP3	NO	
4	NARMSYS	IP	ST2	none	–	–	
5	XIN	IP	XTLI	none	–	–	Xtal In
6	XOUT	OP	–	–	XTLO	NO	Xtal Out
7	TXA	OP	–	–	OP6	NO	
8	TXB	OP	–	–	OP6	NO	
9	RXA	IP	ST2	none	–	–	
10	RXB	IP	ST2	none	–	–	
11	NROM / NC	OP	–	–	OPT6	YES	9
12	NEEPROM / NC	OP	–	–	OPT6	YES	8
13	NSPARE_CS / NC	OP	–	–	OPT6	YES	9
14	V_{DD}	V_{DD}	–	–	–	–	
15	V_{SS}	V_{SS}	–	–	–	–	
16	NRAM / NC	OP	–	–	OP6	NO	10
17	NW0 / NC	OP	–	–	OP6	NO	11
18	NW1 / NC	OP	–	–	OP6	NO	10
19	NW2 / NC	OP	–	–	OP6	NO	10
20	NW3 / NC	OP	–	–	OP6	NO	10
21	NRD / NC	OP		–	OP6	NO	11
22	ARM_ALE / NC	OP	–	–	OP6	NO	8
23	DBE / NC	OP	–	–	OP6	NO	8
24	ACCUM_INT	OP	–	–	OPT1/OPT2	YES	2, 6
25	MEAS_INT	OP	–	–	OPT1/OPT2	YES	2, 7
26	NBW / WRPROG	IP	TTL	none	–	–	
27	NMREQ / DISCIP2	IP	TTL	none	–	–	
28	NOPC / NINTELMOT	IP	TTL	none	–	–	
29	NRW / DISCIP3	IP	TTL	none	–	–	
30	MCLK / NC	OP	–	–	OP6	NO	8
31	ABORT / MICRO_CLK	OP	–	–	OP3	NO	
32	DISCIO	I/O	ST2	none	OPT3	YES	
33	A22 / READ	IP	TTL/ST2	none	–	–	3
34	V_{DD}	V_{DD}	–	–	–	–	
35	V_{SS}	V_{SS}	–	–	–	–	
36	A21 / NCS	IP	TTL/ST2	none	–	–	3
37	A20 / WREN	IP	TTL/ST2	none	–	–	3
38	A9	IP	TTL	none	–	–	
39	A8	IP	TTL	none	–	–	
40	A7	IP	TTL	none	–	–	
41	A6	IP	TTL	none	–	–	
42	A5	IP	TTL	none	–	–	
43	A4	IP	TTL	none	–	–	
44	A3	IP	TTL	none	–	–	

Pin No	Pin Name	Pin Type	Input Type	Pull Up/Dn	O/P Type	Tri-State	Notes
45	A2	IP	TTL	none	–	–	
46	A1 / ALE_IP	IP	TTL/ST2	none	–	–	3
47	A0 / NRESET_IP	IP	TTL/ST2	none	–	–	3
48	D0	I/O	TTL	none	OPT3/OPT6	YES	4, 12
49	D1	I/O	TTL	none	OPT3/OPT6	YES	4, 12
50	D2	I/O	TTL	none	OPT3/OPT6	YES	4, 12
51	D3	I/O	TTL	none	OPT3/OPT6	YES	4, 12
52	D4	I/O	TTL	none	OPT3/OPT6	YES	4, 12
53	D5	I/O	TTL	none	OPT3/OPT6	YES	4, 12
54	D6	I/O	TTL	none	OPT3/OPT6	YES	4, 12
55	V_{DD}	V_{DD}	–	–	–	–	
56	V_{SS}	V_{SS}	–	–	–	–	
57	D7	I/O	TTL	none	OPT3/OPT6	YES	4, 12
58	D8	I/O	TTL	none	OPT3/OPT6	YES	4, 12
59	D9	I/O	TTL	none	OPT3/OPT6	YES	4, 12
60	D10	I/O	TTL	none	OPT3/OPT6	YES	4, 12
61	D11	I/O	TTL	none	OPT3/OPT6	YES	4, 12
62	D12	I/O	TTL	none	OPT3/OPT6	YES	4, 12
63	D13	I/O	TTL	none	OPT3/OPT6	YES	4, 12
64	D14	I/O	TTL	none	OPT3/OPT6	YES	4, 12
65	D15	I/O	TTL	none	OPT3/OPT6	YES	4, 12
66	PLL_LOCK	IP	ST2	none	–	–	
67	V_{DD}	V_{DD}	–	–	–	–	
68	DISCOP	OP	–	–	OPT3	YES	
69	V_{SS}	V_{SS}	–	–	–	–	
70	CLK_T	IP	Diff	none	–	–	
71	CLK_I	IP	Diff	none	–	–	
72	V_{SS}	V_{SS}	–	–	–	–	
73	SAMPCLK	OP	–	–	OP2	No	13
74	V_{DD}	V_{DD}	–	–	–	–	
75	NBRAM / DISCIP4	IP	ST2	none	–	–	
76	SIGN0	IP	ST2/ST1	none	–	–	5, 13
77	MAG0	IP	ST2/ST1	none	–	–	5, 13
78	SIGN1	IP	ST2/ST1	none	–	–	5, 13
79	MAG1	IP	ST2/ST1	none	–	–	5, 13
80	DISCIP1	IP	ST2	none	–	–	

Notes :
1. Although MULTI_FN_IO is capable of being used as a Discrete input, this is not advised since if this pin is driven High at power up, Digital Test Mode will be selected and correct operation will not ensue.
2. Output has power level 1 when OPS_DRIVE_SEL is Low in the SYSTEM_SETUP Register. Output has power level 2 when OPS_DRIVE_SEL is High in the SYSTEM_SETUP Register.
3. Input has TTL thresholds in ARM System mode, but has Schmitt Trigger (type ST2) thresholds in Standard Interface mode.
4. Output has power level 3 when OPS_DRIVE_SEL is Low in the SYSTEM_SETUP Register. Output has power level 6 when OPS_DRIVE_SEL is High in the SYSTEM_SETUP Register.
5. Input has Schmitt Trigger type ST2 thresholds when IPS_3V_MODE is Low in the SYSTEM_SETUP Register. When High they have ST1 thresholds.
6. Usually connected to NFIQ of the ARM60 Processor.
7. Usually connected to NIRQ of the ARM60 Processor.
8. Characterisation data for this pin is with C_L = 10pF.
9. Characterisation data for this pin is with C_L = 20pF.
10. Characterisation data for this pin is with C_L = 30pF
11. Characterisation data for this pin is with C_L = 50pF.
12. Characterisation data for this pin is with C_L = 55pF.
13. Setup and Hold times for the GPS data applied on pins SIGN0, MAG0, SIGN1 and MAG1 are with respect to the rising edge of SAMPCLK. Setup time = 15ns, Hold time = –1ns (i.e. data should not change during the period between 15ns and1ns before the rising edge of SAMPCLK; where SAMPCLK is assumed to be unloaded. The SAMPCLK signal will tend to be further delayed by about 0.1ns / pF of load capacitance).

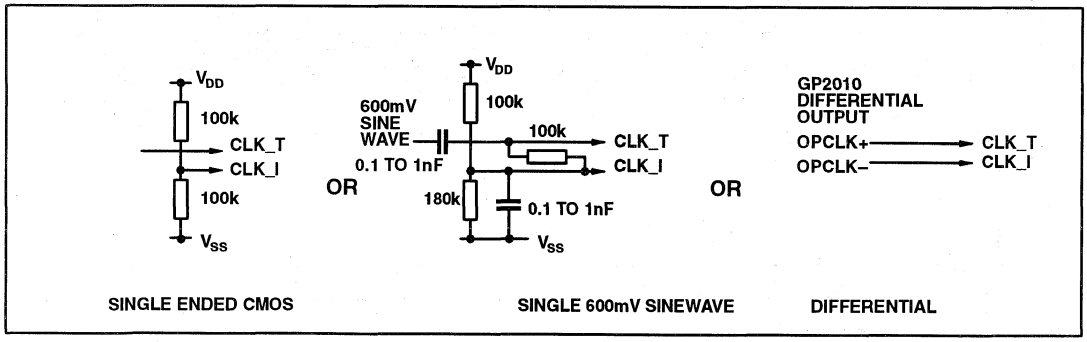


Fig. 24 : Clock interconnect options

TIMING CHARACTERISTICS

Tamb = –40°C to +85°C, V_{DD} = +5.0V ±10%. These characteristics are guaranteed by either production test or design.

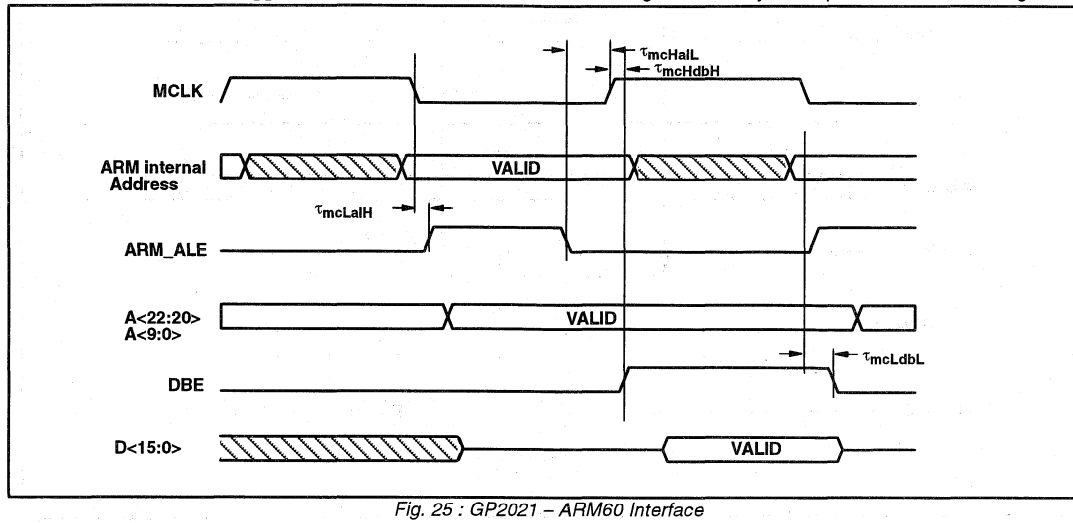


Fig. 25 : GP2021 – ARM60 Interface

Description	Symbol	Min	Max	Units
MCLK Low to ALE High	τ_{mcLalH}	–0.5	0	ns
MCLK High to ALE Low	τ_{mcHalL}	0	0.5	ns
MCLK Low to DBE Low	τ_{mcLdbL}	0.5	1.5	ns
MCLK High to DBE High	τ_{mcHdbH}	0.5	1.5	ns

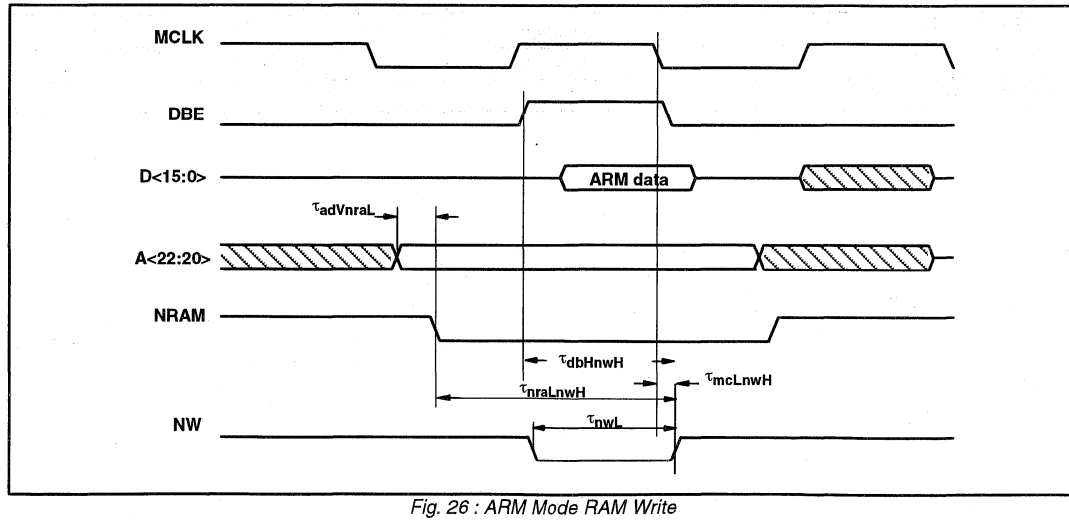


Fig. 26 : ARM Mode RAM Write

Description	Symbol	Min	Max	Units
NRAM Low to NW0–3 High	$\tau_{nraLnwH}$	32	46	ns
MCLK Low to NW0–3 High	τ_{mcLnwH}	0.5	3	ns
DBE High to NW0–3 High	τ_{dbHnwH}	25	27	ns
NW0–3 Low	τ_{nwL}	22	24.5	ns
Address Valid to NRAM Low	$\tau_{adVnraL}$	2	9	ns

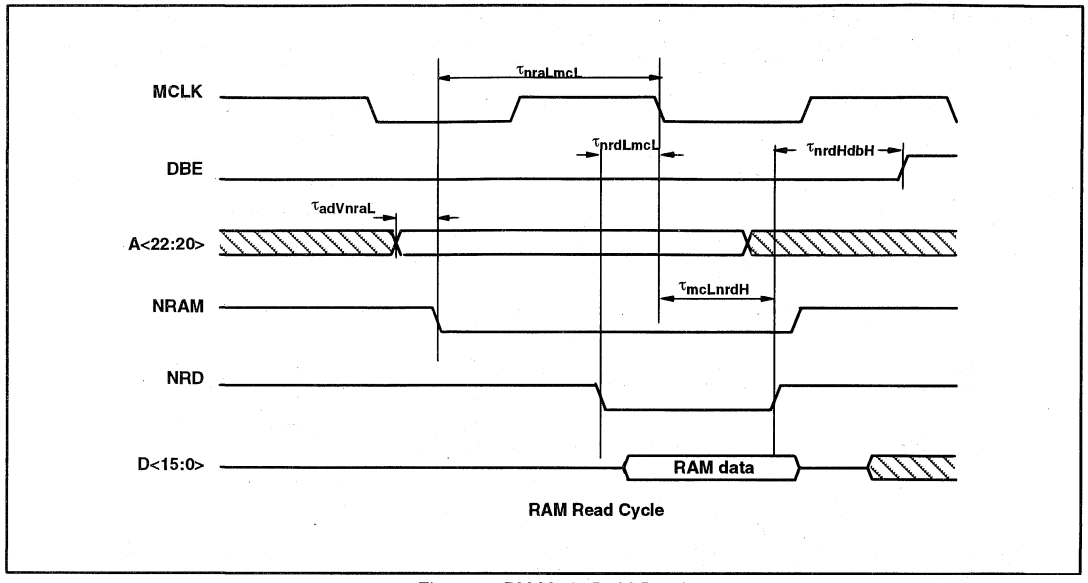


Fig. 27 : ARM Mode RAM Read

Description	Symbol	Min	Max	Units
NRAM Low to MCLK Low	$\tau_{nraLmcL}$	29	45	ns
NRD Low to MCLK Low	$\tau_{nrdLmcL}$	16.5	23	ns
NRD High to DBE High	$\tau_{nrdHdbH}$	15.5	22.5	ns
MCLK Low to NRD High	$\tau_{mcLnrdH}$	2.5	11.5	ns
Address Valid to NRAM Low	$\tau_{adVnraL}$	2	8	ns

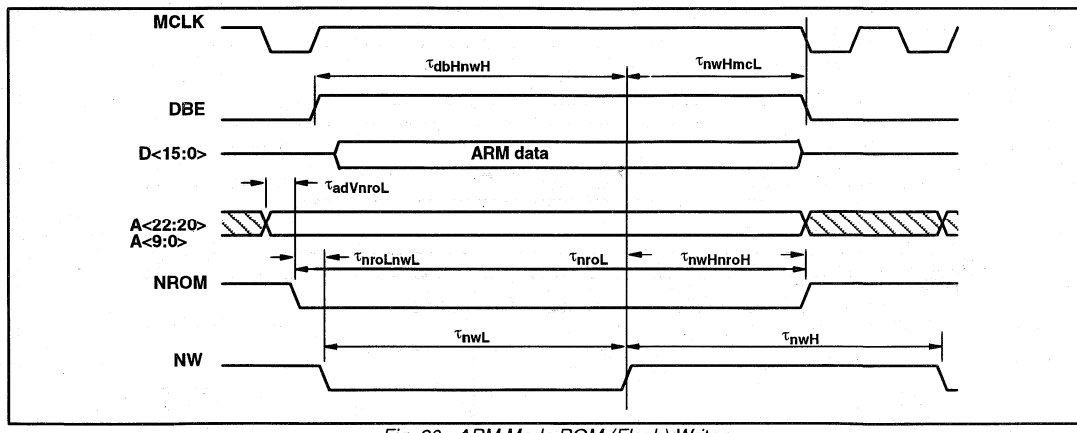


Fig. 28 : ARM Mode ROM (Flash) Write

Description	Symbol	Min	Max	Units	Notes
NROM Low	τ_{nroL}	100		ns	1
NROM Low to NW0–3 Low	$\tau_{nroLnwL}$	11	21.5	ns	
DBE High to NW0–3 High	τ_{dbHnwH}	52	57	ns	1
NW0–3 Low	τ_{nwL}	50	51	ns	1
NW0–3 High to MCLK Low	τ_{nwHmcL}	16	23	ns	
NW0–3 High to NROM High	$\tau_{nwHnroH}$	27.5	39	ns	
NW0–3 High	τ_{nwH}	47	49	ns	
Address Valid to NROM Low	$\tau_{adVnroL}$	2	7.5	ns	

Note: 1. +50ns / extra wait state

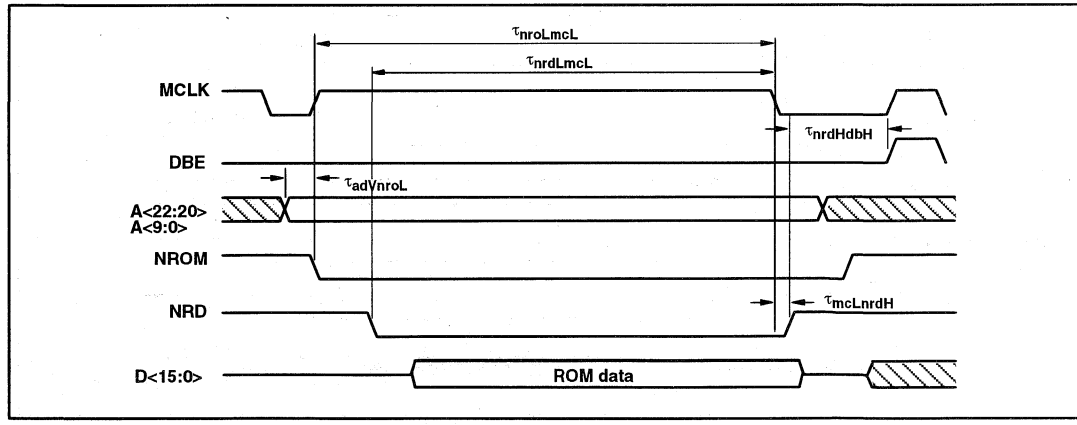


Fig. 29 : ARM Mode ROM Read

Description	Symbol	Min	Max	Units	Notes
NROM Low to MCLK Low	$\tau_{nroLmcL}$	48	74.5	ns	1
NRD Low to MCLK Low	$\tau_{nrdLmcL}$	48	50	ns	1
NRD High to DBE High	$\tau_{nrdHdbH}$	33	45	ns	
MCLK Low to NRD High	$\tau_{mcLnrdH}$	2.5	10	ns	
Address Valid to NROM Low	$\tau_{adVnroL}$	2.5	9	ns	

Note: 1. +50ns / extra wait state

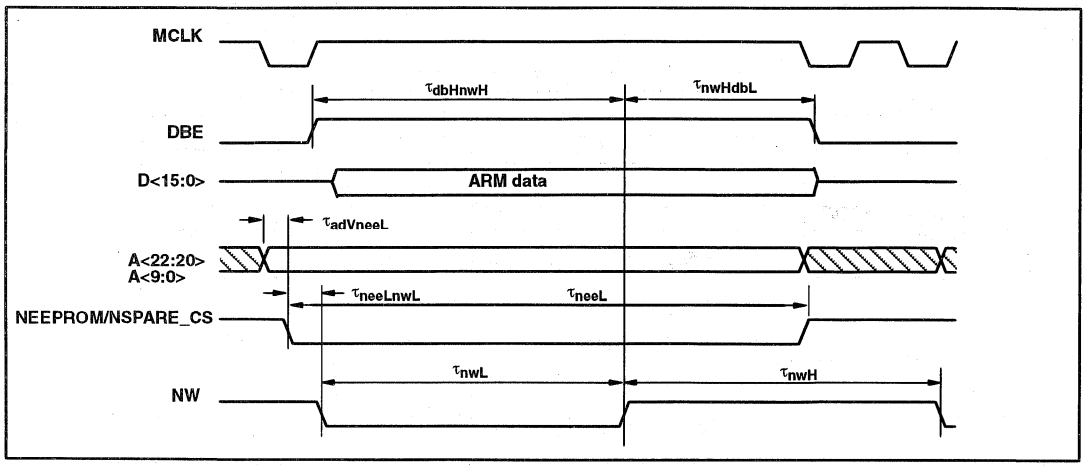


Fig. 30 : ARM Mode EEPROM write

Description	Symbol	Min	Max	Units
NEEPROM Low	τ_{neeL}	348		ns
NEEPROM Low to NW0–3	$\tau_{neeLnwL}$	11		ns
NW0–3 Low	τ_{nwL}	150		ns
NW0–3 High	τ_{nwH}	200		ns
DBE High to NW0–3 High	τ_{dbHnwH}	150		ns
NW0–3 High to DBE Low	τ_{nwHdbL}	168		ns
Address Valid to NEEPROM Low	$\tau_{adVneeL}$	2.5	9	ns

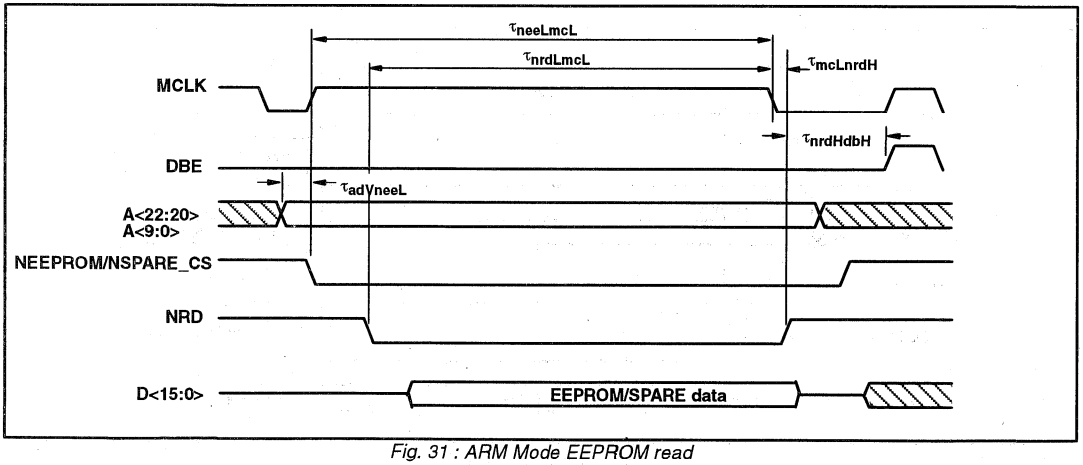


Fig. 31 : ARM Mode EEPROM read

Description	Symbol	Min	Max	Units	Notes
NEEPROM Low to MCLK Low	$\tau_{neeLmcL}$	124.5		ns	1
NRD Low to MCLK Low	$\tau_{nrdLmcL}$	117		ns	1
NRD High to DBE High	$\tau_{nrdHdbH}$	65		ns	
MCLK Low to NRD High	$\tau_{mcLnrdH}$	2.5	10	ns	
Address Valid to NEEPROM Low	$\tau_{adVneeL}$	2.5	9	ns	

Notes: 1. +50ns / extra wait state.

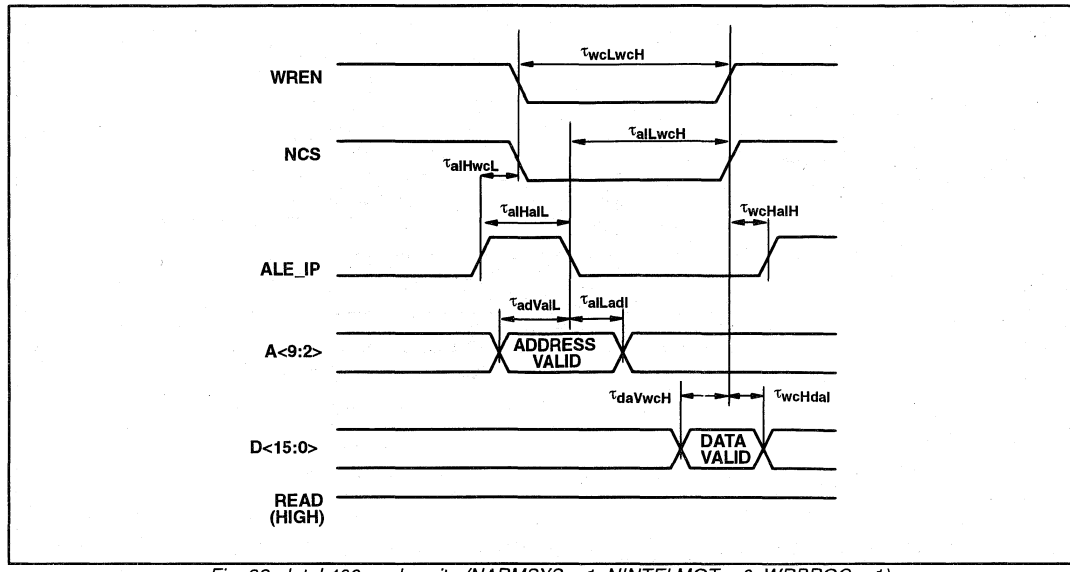


Fig. 32 : Intel 486 mode write (NARMSYS = 1, NINTELMOT = 0, WRPROG = 1)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
ALE_IP High to WREN and NCS Low setup time	τ_{alHwcL}	5		ns	
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	13		ns	
ALE_IP Low to WREN or NCS High pulse width	τ_{alLwcH}	10		ns	1
WREN and NCS Low to WREN or NCS High pulse width	τ_{wcLwcH}	10		ns	
WREN or NCS High to ALE_IP High hold–off time	τ_{wcHalH}	5		ns	
Address Valid to ALE_IP Low setup time	τ_{adValL}	9		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadI}	8		ns	
Data Valid to WREN or NCS High setup time	τ_{daVwcH}	7		ns	
WREN or NCS High to Data Invalid hold time	τ_{wcHdaI}	5		ns	

Note: 1 Write inhibited until ALE_IP falling edge.

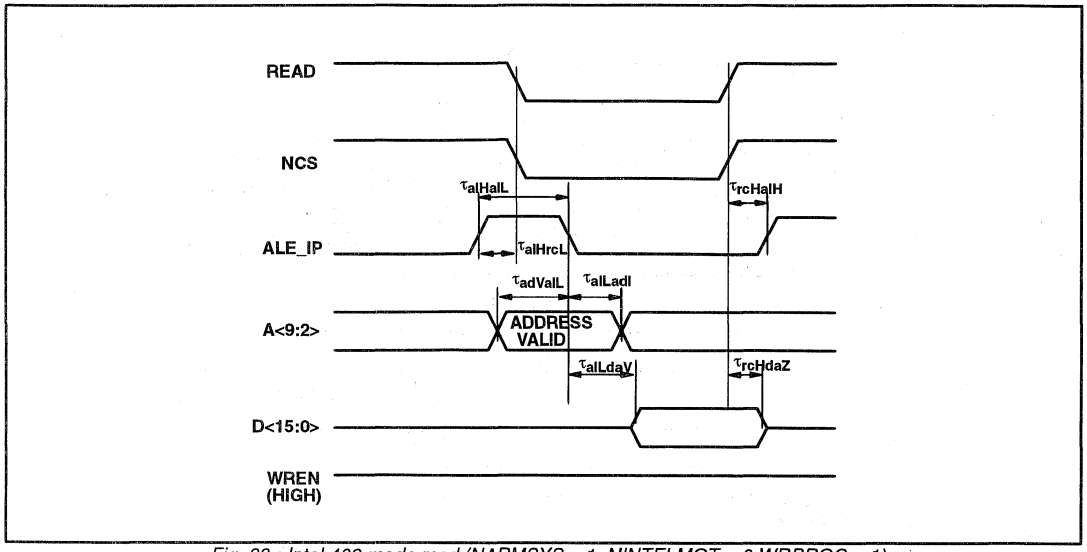


Fig. 33 : Intel 486 mode read (NARMSYS = 1, NINTELMOT = 0,WRPROG = 1)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
ALE_IP High to READ and NCS Low setup time	τ_{alHrcL}	5		ns	
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	13		ns	
READ or NCS High to ALE_IP High hold–off time	τ_{rcHalH}	5		ns	
Address Valid to ALE_IP Low setup time	τ_{adValL}	9		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadI}	8		ns	
ALE_IP Low to Data Valid propagation delay	τ_{alLdaV}		44	ns	1,2,3
READ or NCS High to Data High Impedance	τ_{rcHdaZ}	4	23	ns	

Notes: 1 Read inhibited until ALE_IP falling edge.

2 The ALE_IP Low to Data Output Valid Delay assumes ALE_IP is overlapping the READ and NCS Low time. If not, the τ_{alLdaV} parameter applies from the point at which both READ and NCS are Low.

3. The Data Out Propagation delay is for a data bus load of 50pF.

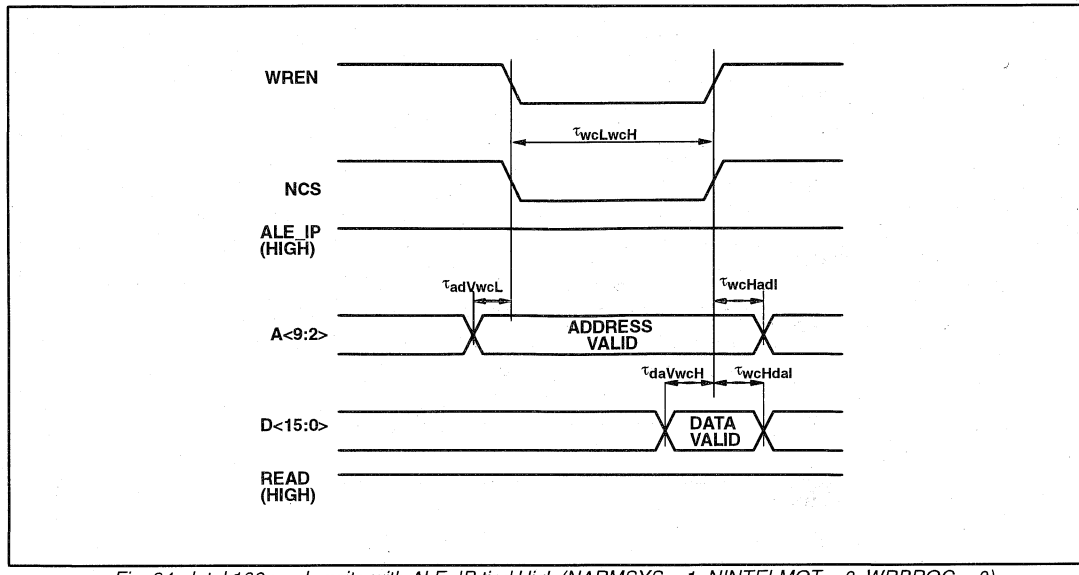


Fig. 34 : Intel 186 mode write with ALE_IP tied High (NARMSYS = 1, NINTELMOT = 0, WRPROG = 0)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN and NCS Low to WREN or NCS High pulse width	τ_{wcLwcH}	10		ns	
Address valid to WREN and NCS Low setup time	τ_{adVwcL}	9		ns	
WREN or NCS High to Address Invalid Hold time	τ_{wcHadI}	10		ns	
Data Valid to WREN or NCS High setup time	τ_{daVwcH}	7		ns	
WREN or NCS High to Data Invalid hold time	τ_{wcHdaI}	5		ns	

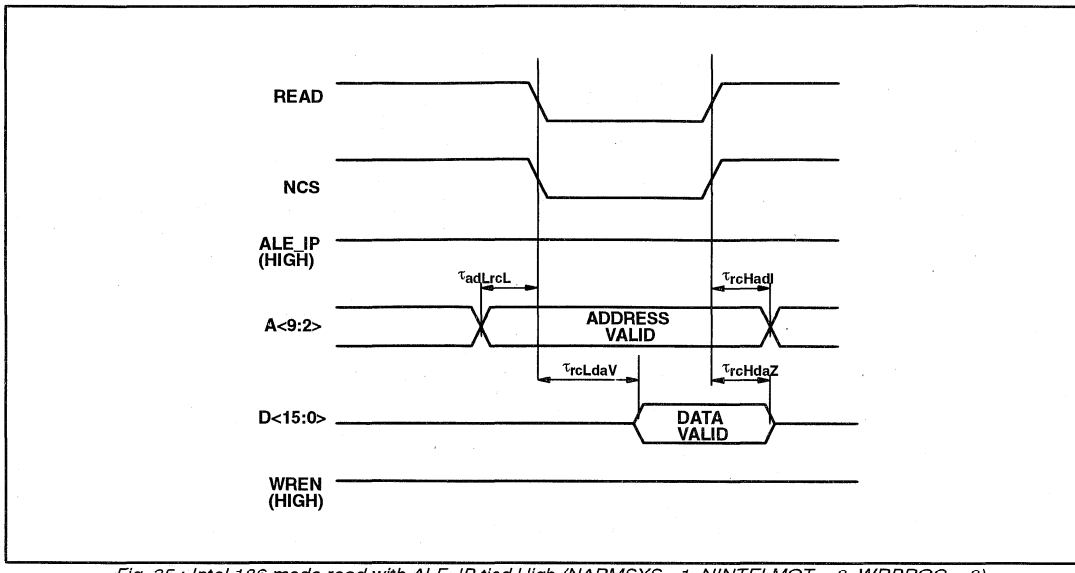


Fig. 35 : Intel 186 mode read with ALE_IP tied High (NARMSYS =1, NINTELMOT = 0, WRPROG = 0)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
Address Valid to READ and NCS Low setup time	τ_{adVrcL}	9		ns	
READ or NCS High to Address Invalid hold time	τ_{rcHadI}	10		ns	
READ and NCS Low to Data Valid propagation delay	τ_{rcLdaV}		44	ns	1
READ or NCS High to Data High Impedance	τ_{rcHdaZ}	4	23	ns	

Notes: 1 The Data Out Propagation delay is for a Data Bus load of 50pF.

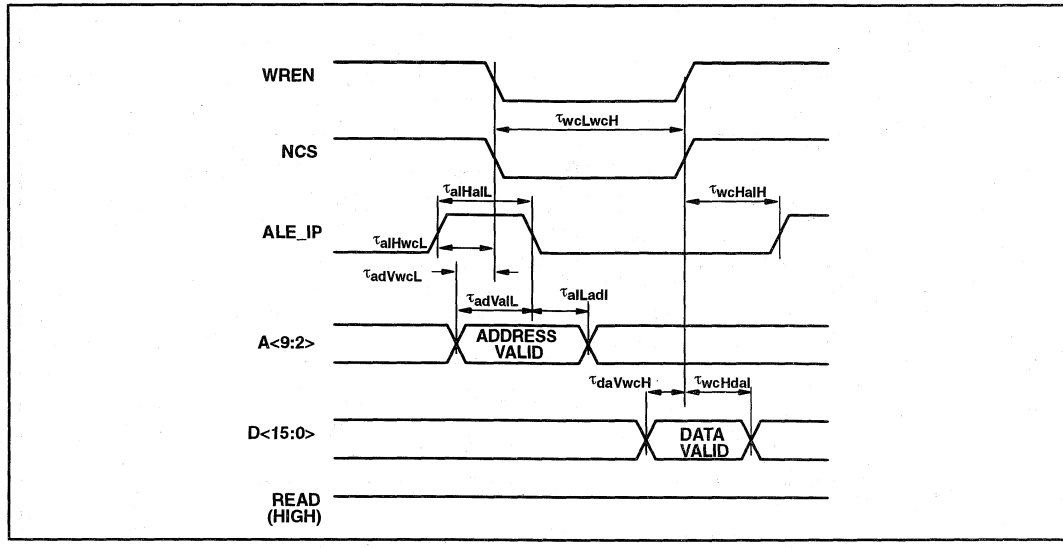


Fig. 36 : Intel 186 mode write, ALE_IP being pulsed (NARMSYS = 1, NINTELMOT = 0, WRPROG = 0)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
ALE_IP High to WREN and NCS Low setup time	τ_{alHwcL}	14		ns	
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	10		ns	
WREN and NCS Low to WREN or NCS High pulse width	τ_{wcLwcH}	10		ns	
WREN or NCS High to ALE_IP High hold off time	τ_{wcHalH}	5		ns	
Address Valid to WREN and NCS Low setup time	τ_{adVwcL}	10		ns	
Address Valid to ALE_IP Low setup time	τ_{adValL}	8		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadI}	8		ns	
Data Valid to WREN or NCS High setup time	τ_{daVwcH}	7		ns	
WREN or NCS High to Data Invalid hold time	τ_{wcHdaI}	5		ns	

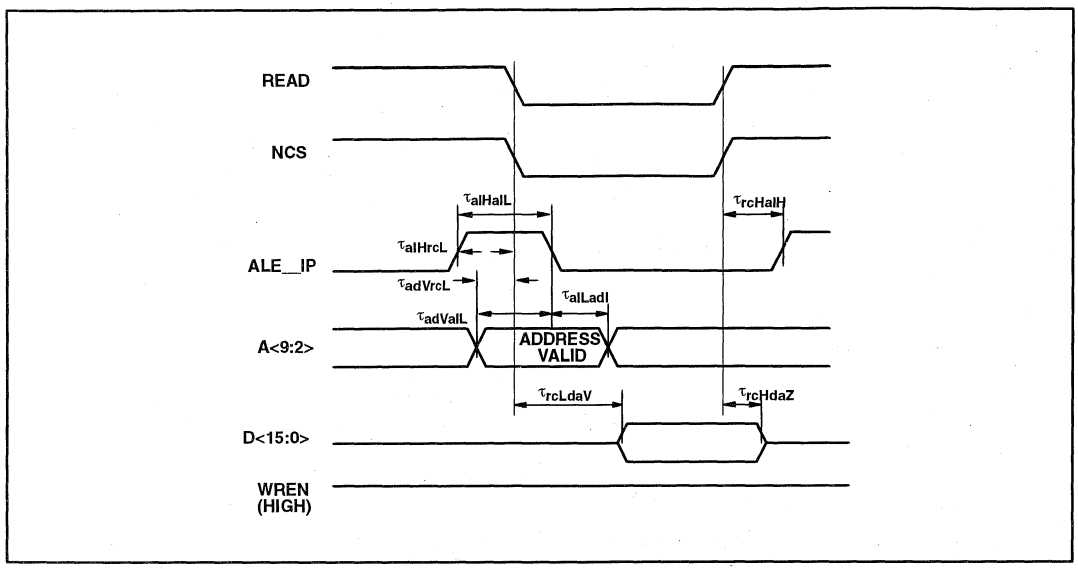


Fig. 37 : Intel 186 mode read, ALE_IP being pulsed. (NARMSYS = 1, NINTELMOT = 0, WRPROG = 0)

Timing Parameter Description	Symbol	Min	Max	Units	Units
ALE_IP High to READ and NCS Low setup time	τ_{alHrcL}	14		ns	
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	10		ns	
READ or NCS High to ALE_IP High hold off time	τ_{rcHalH}	5		ns	
Address Valid to READ and NCS Low setup time	τ_{adVrcL}	10		ns	
Address Valid to ALE_IP Low setup time	τ_{adValL}	8		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadI}	8		ns	
READ and NCS Low to Data Valid propagation delay	τ_{rcLdaV}		44	ns	1
READ or NCS High to Data High Impedance	τ_{rcHdaZ}	4	23	ns	

Notes: 1 The Data Out propagation delay is for a Data Bus load of 50pF.

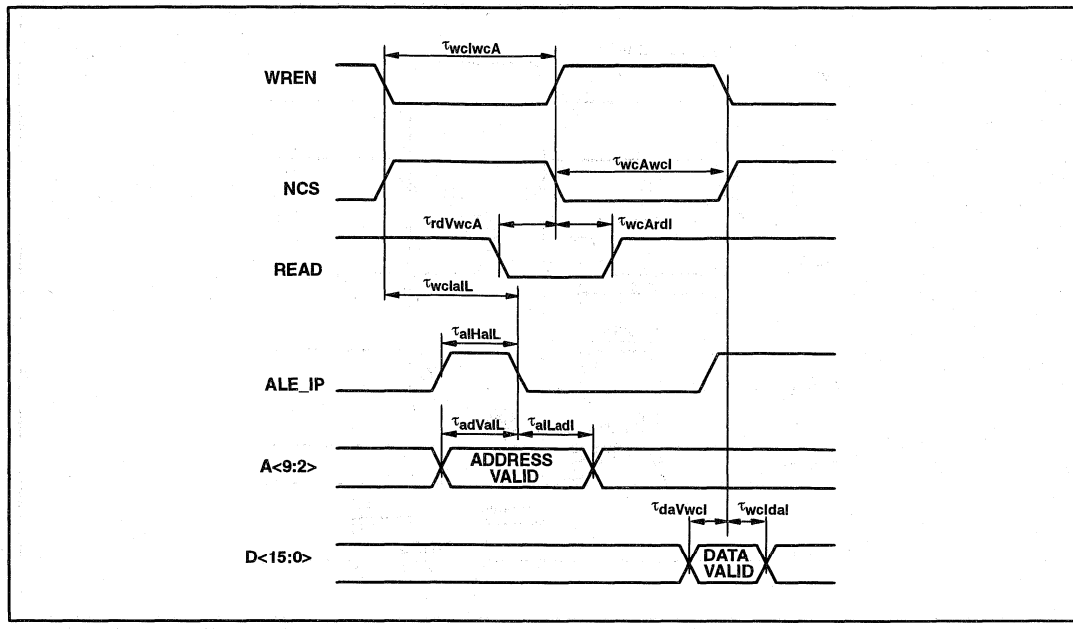


Fig. 38 : Motorola mode write, ALE_IP non–overlapping WREN and NCS (NARMSYS = 1, NINTELMOT = 1, WRPROG = X)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN or NCS Inactive to WREN and NCS active	τ_{wclwcA}	23		ns	1
WREN and NCS active to WREN or NCS inactive	τ_{wcAwcl}	10		ns	1
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	13		ns	
WREN or NCS Inactive to ALE_IP Low Hold off time	τ_{wclalL}	23		ns	1
Address Valid to ALE_IP Low setup time	τ_{adValL}	9		ns	
ALE_IP Low to Address Invalid hold time	τ_{alLadl}	8		ns	
READ Valid to WREN and NCS Active setup time	τ_{rdVwcA}	7		ns	1, 2
WREN and NCS Active to READ Invalid hold time	τ_{wcArdl}	5		ns	1, 2
DATA Valid to WREN or NCS Inactive setup time	τ_{daVwcl}	7		ns	1
WREN or NCS Inactive to DATA Invalid hold time	τ_{wcldal}	5		ns	1

Notes: 1 WREN is active High, NCS is Active Low.
2 READ is transparently latched by WREN and NCS being active.
3 There is no parameter specified for WREN or NCS Inactive to ALE_IP High, since the internal ALE signal is disabled until after the end of the internal Read or Write Strobe; hence the need for the τ_{wclalL} parameter.

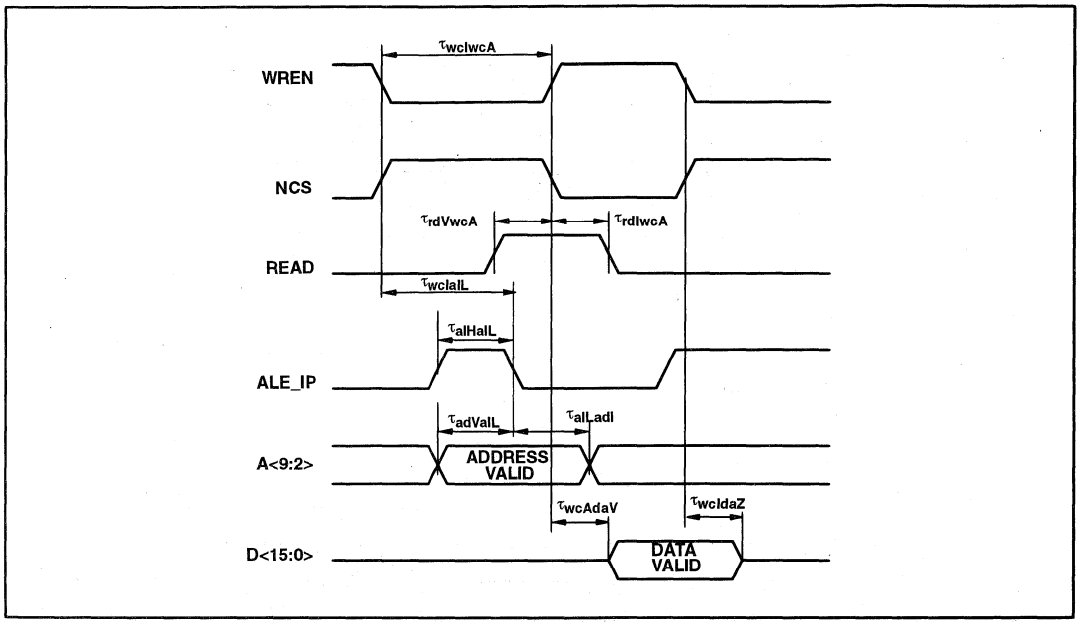


Fig. 39 : Motorola mode read, ALE_IP non–overlapping WREN and NCS (NARMSYS = 1, NINTELMOT = 1, WRPROG = X)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN or NCS Inactive to WREN and NCS active	τ_{wclwcA}	23		ns	1
ALE_IP High to ALE_IP Low pulse width	τ_{alHalL}	13		ns	
WREN or NCS Inactive to ALE_IP Low Hold off time	τ_{wclalL}	23		ns	1
Address Valid to ALE_IP Low setup time	τ_{adValL}	9		ns	
ALE_IP Low to Address Invalid Hold time	τ_{alLadI}	8		ns	
READ Valid to WREN and NCS Active setup time	τ_{rdVwcA}	7		ns	1, 2
WREN and NCS Active to READ Invalid Hold time	τ_{wcArdI}	5		ns	1, 2
WREN or NCS Active to DATA valid	τ_{wcAdaV}		44	ns	1
WREN or NCS Inactive to DATA High impedance	τ_{wcldaZ}	4	23	ns	1

Notes: 1 WREN is active High, NCS is active Low.
2 READ is transparently latched by WREN and NCS being active.
3 There is no parameter specified for WREN or NCS Inactive to ALE_IP High, since the internal ALE signal is disabled until after the end of the internal Read or Write Strobe; hence the need for the τ_{wclalL} parameter.

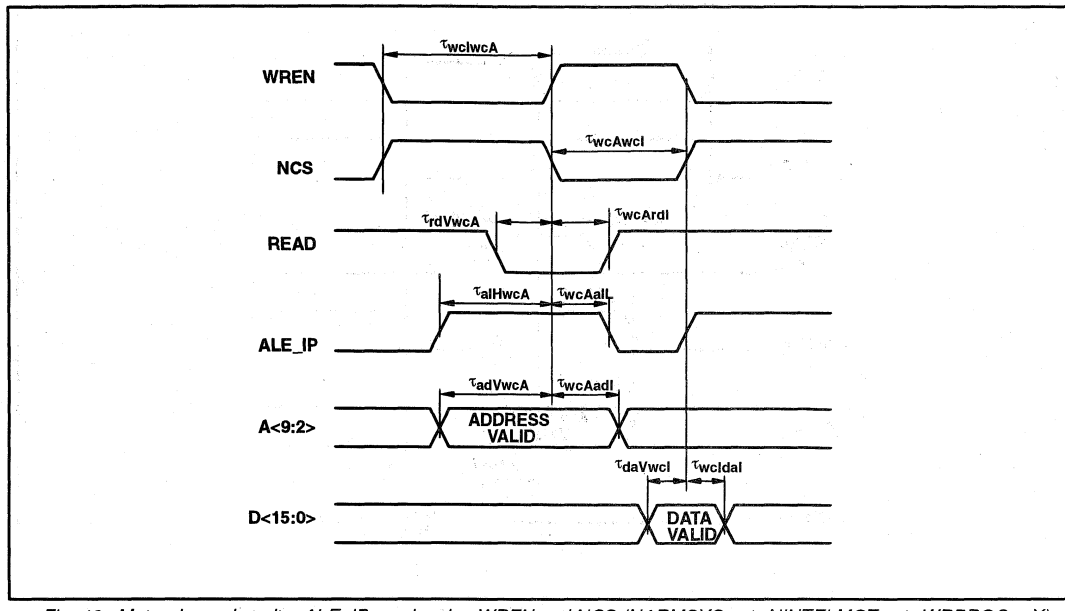


Fig. 40 : Motorola mode write, ALE_IP overlapping WREN and NCS (NARMSYS = 1, NINTELMOT = 1, WRPROG = X)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN or NCS Inactive to WREN and NCS active	τ_{wclwcA}	23		ns	1
WREN and NCS Active to WREN or NCS inactive	τ_{wcAwcl}	10		ns	1
ALE_IP High to WREN and NCS Active pulse width	τ_{alHwcA}	13		ns	1
WREN and NCS Active to ALE_IP Low hold time	τ_{wcAalL}	6		ns	1, 2
Address Valid to WREN and NCS Active setup time	τ_{adVwcA}	9		ns	1
WREN and NCS Active to Address Invalid hold time	τ_{wcAadl}	11		ns	1
READ Valid to WREN and NCS Active setup time	τ_{rdVwcA}	7		ns	1, 3
WREN and NCS Active to READ Invalid hold time	τ_{wcArdl}	5		ns	1, 3
DATA Valid to WREN or NCS Inactive setup time	τ_{daVwcl}	7		ns	1
WREN or NCS Inactive to DATA Invalid hold time	τ_{wcldal}	5		ns	1

Notes: 1 WREN is active High, NCS is Active Low.
2 If ALE_IP does not overlap WREN and NCS active by τ_{wcAalL} then the timings for ALE_IP both overlapping and non–overlapping WREN and NCS active must be met.
3 READ is transparently latched by WREN and NCS being active.
4 There is no parameter specified for WREN or NCS Inactive to ALE_IP High, since the internal ALE signal is disabled until after the end of the internal Read or Write Strobe; hence the need for the τ_{wclalL} parameter.

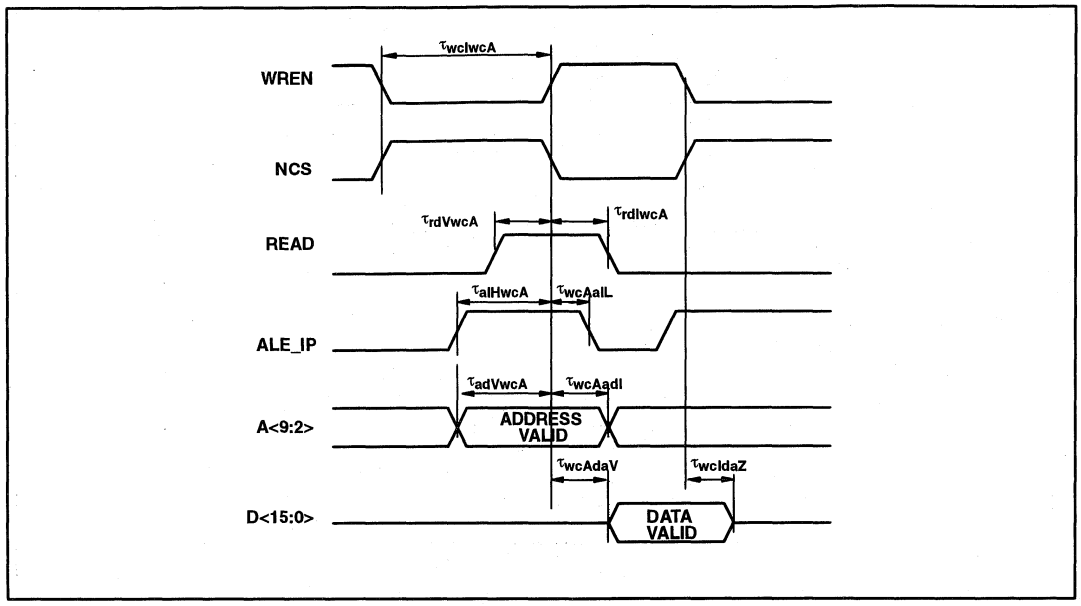


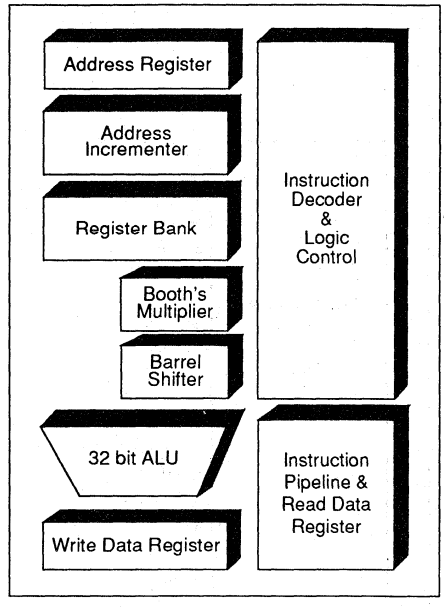
Fig. 41 : Motorola mode read, ALE_IP overlapping WREN and NCS (NARMSYS = 1, NINTELMOT = 1, WRPROG = X)

Timing Parameter Description	Symbol	Min	Max	Units	Notes
WREN or NCS Inactive to WREN and NCS active	τ_{wclwcA}	23		ns	1
ALE_IP High to WREN and NCS Active pulse width	τ_{alHwcA}	13		ns	1
WREN or NCS Active to ALE_IP Low hold time	τ_{wcAalL}	6		ns	1,2
Address Valid to WREN and NCS Active setup time	τ_{adVwcA}	9		ns	1
WREN and NCS Active to Address Invalid hold time	τ_{wcAadl}	11		ns	1
READ Valid to WREN and NCS Active setup time	τ_{rdVwcA}	7		ns	1, 3
WREN and NCS Active to READ Invalid hold time	τ_{wcArdl}	5		ns	1, 3
WREN or NCS Active to DATA valid	τ_{wcAdaV}		44	ns	1
WREN or NCS Inactive to DATA High impedance	τ_{wcldaZ}	4	23	ns	1

Notes:
1 WREN is active High, NCS is Active Low.
2 If ALE_IP does not overlap WREN and NCS active by τ_{wcAalL} then the timings for ALE_IP both overlapping and non–overlapping WREN and NCS active must be met.
3 READ is transparently latched by WREN and NCS being active.
4 There is no parameter specified for WREN or NCS Inactive to ALE_IP High, since the internal ALE signal is disabled until after the end of the internal Read or Write Strobe; hence the need for the τ_{wclalL} parameter.

ARM60-B RISC Processor

The ARM60-B is a low power, general purpose 32-bit RISC microprocessor. It is an implementation of the ARM6 macrocell, packaged in a compact 100 pin Metric Quad Flat Pack. Its simple, elegant and fully static design is particularly suitable for cost and power sensitive applications.



- **32 bit RISC processor**
- **32 bit data bus**
- **32 bit address bus**
- **Big and Little Endian operating modes**
- **High performance RISC**
  27 Dhrystone MIPS @ 5V/30MHz
- **Temperature range -40°C to +85°C**
- **Low power consumption**
  1.2mA/MHz @ 5V fabricated in 0.6µm CMOS
- **Fully static operation**
  ideal for power sensitive applications
- **Fast interrupt response**
  for real-time applications
- **Virtual Memory System Support**
- **Excellent high-level language support**
- **Simple but powerful instruction set**
- **IEEE 1149.1 (JTAG) Boundary Scan**
  to ease testing

Applications:

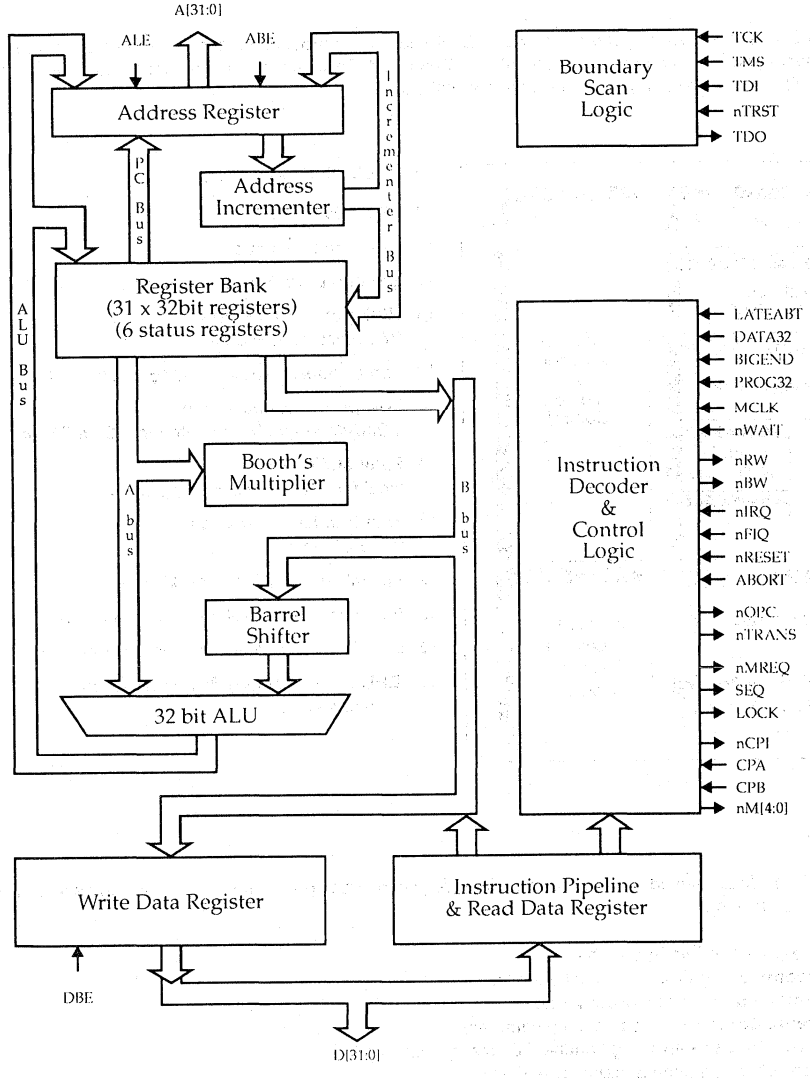
The ARM60-B is ideally suited to those applications requiring RISC performance from a compact, power efficient processor. These include:

Global Positioning Systems
Telecomms - eg GSM terminal controller
Datacomms - eg protocol conversion
Portable Computing - eg palmtop computer
Portable Instruments - eg handheld data acquisition unit
Automotive - eg engine management unit
Information Systems - eg smart cards
Consumer Multimedia - low cost controller

Ordering Code
P60ARM-B/IG/GPFR

For full details please contact your local GEC Plessey Semiconductors Customer Service Centres

GEC PLESSEY
SEMICONDUCTORS


A[31:0]
ALE
ABE
Address Register
Address Incrementer
Incrementer Bus
PC Bus
Register Bank
(31 x 32bit registers)
(6 status registers)
ALU Bus
Booth's Multiplier
A bus
B bus
Barrel Shifter
32 bit ALU
Boundary Scan Logic
TCK
TMS
TDI
nTRST
TDO
Instruction Decoder & Control Logic
LATEABT
DATA32
BIGEND
PROG32
MCLK
nWAIT
nRW
nBW
nIRQ
nFIQ
nRESET
ABORT
nOPC
nTRANS
nMREQ
SEQ
LOCK
nCPI
CPA
CPB
nM[4:0]
Write Data Register
Instruction Pipeline & Read Data Register
DBE
D[31:0]

Section 4
Development Systems

GEC PLESSEY
SEMICONDUCTORS

GPS*Builder-2*

12 CHANNEL GPS DEVELOPMENT SYSTEM

(Supersedes GPSBuilder™, DS4004 - 1.2, July 1994)

The GPS*Builder-2* 12 channel GPS Development System comprises hardware and GPS tracking and navigation software for a 486 PC platform, transforming the PC into a learning tool and prototyping aid for designers of Global Positioning System (GPS) receivers.

FEATURES

- 12 channel GPS Receiver architecture,
- 486-PC ISA bus compatible plug-in card,
- Source Code files (in 'C') included,
- Non restrictive Software license,
- Removable RF/Correlator daughter board,
- Active patch antenna and 10 meter (33 feet) cable,
- Differential GPS capability,
- Comprehensive manual with software flow charts.

The GPS*Builder-2* allows functional demonstration of 12 independent satellite channels using a 486 DX personal computer. The antenna (which must be located externally) is provided as part of the kit. All satellite tracking and navigation software is supplied in DOS-executable code, and all software source files (written in 'C') are included.

The GPS*Builder-2* uses integrated circuits manufactured by GEC Plessey Semiconductors. The chip set comprises the GP2010 RF downconverter, 35.4MHz IF SAW filter (part number DW9255) and a GP2021 correlator IC. The GP2021 12-channel correlator operates under host PC microprocessor control across the 16 bit ISA bus.

The circuit has been partitioned so that the downconverter, correlator, the 10 MHz TCXO and all other components are contained on a daughter board mounted to the expansion card (see figure 1). The daughter board can be easily removed from the expansion card and connected to a different processor directly if necessary.

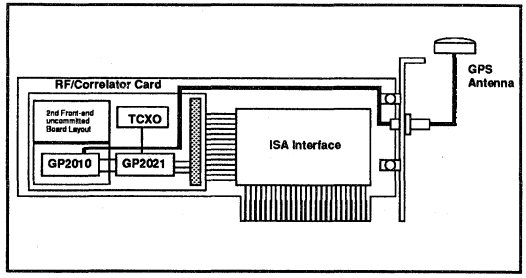


Fig.1 GPSBuilder-2 ISA Plug-in Card

Two serial ports are provided, giving I/O access to registers within the GP2021, under software control.

The software core routines acquire and track satellites using each of the 12 independent tracking channels in the GP2021 correlator, then compute a position solution from the resulting data. The results of this process are shown on various display screens on the PC monitor.

The primary display screen is the channel status view (see figure 2). This display provides a continuously updating view of all the correlation channels and the navigation solution. Other screens display information such as satellite status, processing and task status, differential correction status and control of RINEX2 data collection. These views can be accessed under function-key control. This information will help the user who has limited experience of GPS receiver design to understand basic operation, and the experienced designer will be able to monitor the effects of modifying the underlying algorithms within the GPS software.

The software has been written in 'C' and compiled for a PC with an 80386/486 microprocessor. Within the source code files, all routines are well-commented for ease of understanding. GPS*Builder-2* includes a licence to modify the software and distribute it in embedded form. This source code can be recompiled using Borland C++ rev 3.1 or 4.0.

GPS*Builder-2* software has not been optimised for a particular microprocessor or GPS application so modifications to the underlying algorithms and program code may or may not be required depending on use. In some applications, code optimisation will almost certainly be required to reduce the processing requirements (and hence the cost of the processor hardware). GEC Plessey Semiconductors does not offer technical support in making such changes.

RELATED PRODUCTS

Part No	Description	Data Sheet Reference
DW9255	35.42 MHz SAW Filter	DS3861
GP2010	GPS RF Front End	DS4056
GP2021	12 Channel Correlator	DS4057

ORDERING CODES

Full GPS*Builder-2* System:

GPSBD2PDLC/11/SOFT

GPS*Builder-2* hardware (excludes software):

GPSBD2PDV2/RR/HARD

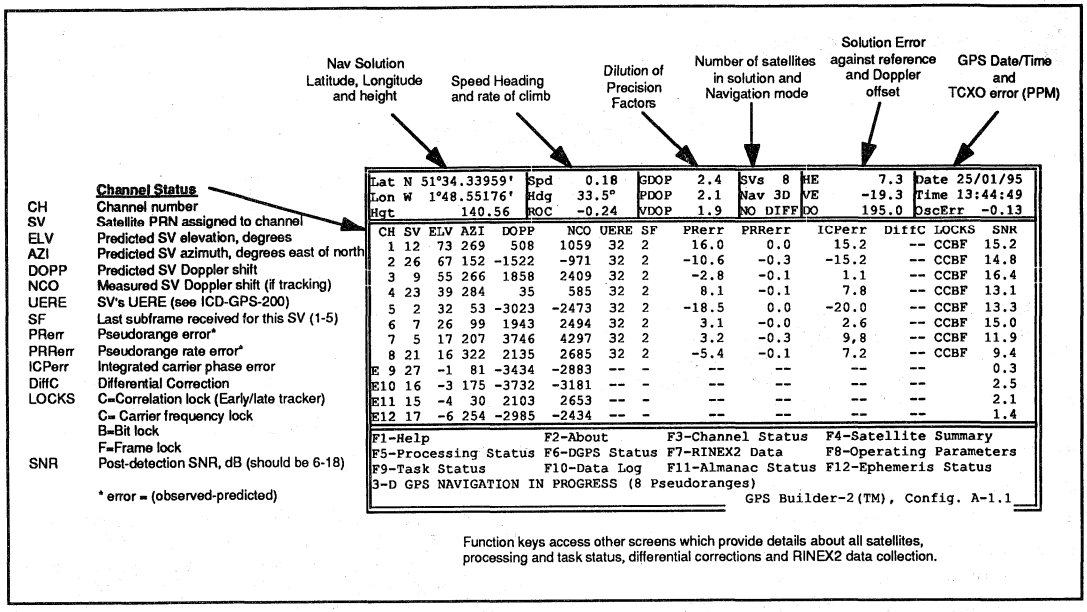


Fig.2 GPSBuilder-2 Channel Status Screen

Host Computer Requirements

IBM PC Compatible
MS-DOS Rev 5.0 or higher
80486 DX CPU, 33MHz or faster (for 12 channel operation)
Serial Port (for differential capability)
Borland C++ compiler, Rev 3.1 or 4.0*

* to recompile the source code.

Note: We do not provide technical support of changes made to the product as supplied

GPS*Builder-2* kit contents

PC ISA bus interface card
RF/Correlator daughter board
Active Antenna (gain: 26dB, NF <2.5dB) with SMA side-mounted connector. Magnetic mount
10 meters (33 feet) antenna cable with SMA connectors
Software on 3.5 inch HD diskette
Operating Manual with schematics, flow charts and tutorial,
Software license agreement

GPS*Builder-2.1*

12 CHANNEL GPS DEVELOPMENT SYSTEM

(Complements GPSBuilder-2, DS4004)

The GPS*Builder-2.1* 12 channel GPS Development System comprises hardware and GPS tracking and navigation software for an IBM compatible PC platform, transforming the PC into a learning tool and prototyping aid for designers of Global Positioning System (GPS) receivers.

FEATURES

- 12 channel GPS Receiver architecture,
- ISA bus compatible plug-in card,
- Source Code files (in 'C') included,
- Non restrictive Software license,
- Active patch antenna and 10 meter (33 feet) cable,
- Differential GPS capability,
- Comprehensive manual with software flow charts.

GPS*Builder-2.1* allows functional demonstration of 12 independent satellite channels using an IBM compatible personal computer. The antenna (which must be located externally) is provided as part of the kit. All satellite tracking and navigation software is supplied in DOS-executable code, and all software source files (written in 'C') are included.

GPS*Builder-2.1* uses integrated circuits manufactured by GEC Plessey Semiconductors. The chip set comprises the GP2015 RF downconverter, a 35.4MHz IF SAW filter (part number DW9255) and a GP2021 correlator IC. GP2021 12-channel correlator operates under host PC microprocessor control across the 16 bit ISA bus.

GPS*Builder-2.1* complements GPS*Builder-2*. With GPS*Builder-2.1*, all the components are mounted on a single, half-size card, making it suitable for a wide range of PCs. It also uses the GP2015 RF front end IC. If greater flexibility is required, the original GPS*Builder-2* uses a full length card with a removable daughterboard. The front end chip on the daughterboard is a GP2010.

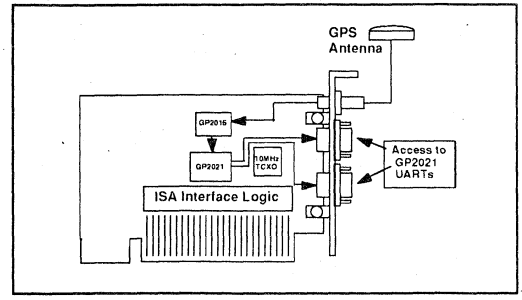


Fig.1 GPSBuilder-2.1 ISA Plug-in Card

Two serial ports are provided, giving I/O access to registers within the GP2021, under software control.

The software core routines acquire and track satellites using each of the 12 independent tracking channels in the GP2021 correlator, then compute a position solution from the resulting data. The results of this process are shown on various display screens on the PC monitor.

The primary display screen is the channel status view (see figure 2). This display provides a continuously updating view of all the correlation channels and the navigation solution. Other screens display information such as satellite status, processing and task status, differential correction status and control of RINEX2 data collection. These views can be accessed under function-key control. This information will help the user who has limited experience of GPS receiver design to understand basic operation, and the experienced designer will be able to monitor the effects of modifying the underlying algorithms within the GPS software.

The software has been written in 'C' and compiled for a PC with an 80486 or Pentium microprocessor. Within the source code files, all routines are well-commented for ease of understanding. GPS*Builder-2.1* includes a licence to modify the software and distribute it in embedded form. This source code can be recompiled using Borland C++ rev 3.1 or 4.0.

GPS*Builder-2.1* software has not been optimised for a particular microprocessor or GPS application so modifications to the underlying algorithms and program code may or may not be required depending on use. In some applications, code optimisation will almost certainly be required to reduce the processing requirements (and hence the cost of the processor hardware). GEC Plessey Semiconductors does not offer technical support in making such changes.

RELATED PRODUCTS

Part No	Description	Data Sheet Reference
DW9255	35.42 MHz SAW Filter	DS3861
GP2015	GPS RF Front End	DS4374
GP2021	12 Channel Correlator	DS4057

ORDERING CODES

Full GPS*Builder-2.1* System:
GPSBUILDER/21/SSTM

GPS*Builder-2.1* hardware only:
GPSBUILDER/21/HARD

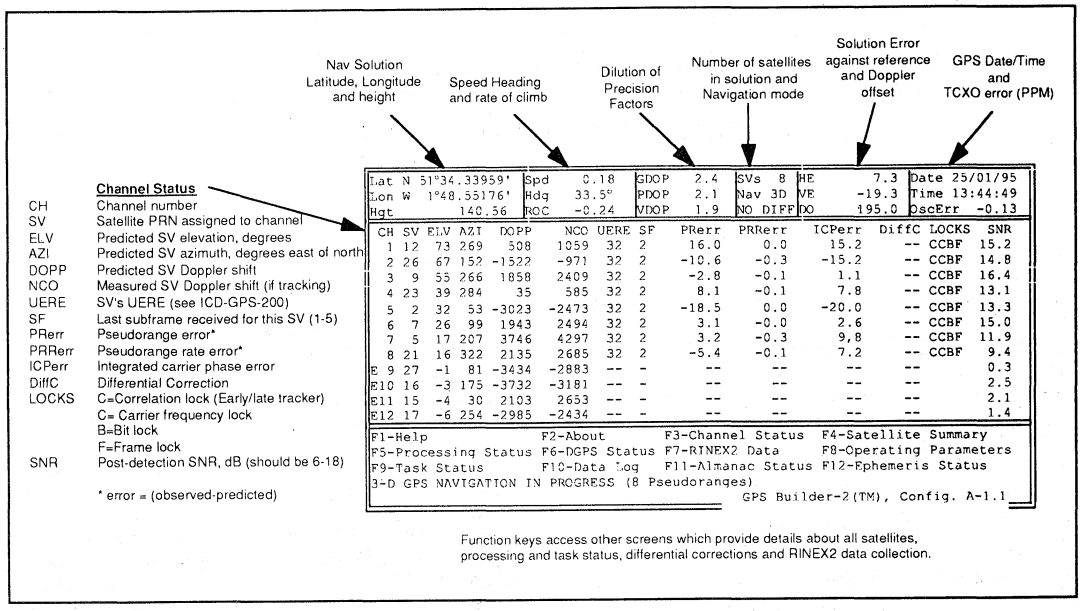


Fig.2 GPSBuilder-2.1 Channel Status Screen

Host Computer Requirements

IBM PC Compatible
MS-DOS Rev 5.0 or higher
80486 DX or Pentium CPU, 50MHz or faster (for 12 channel operation)
Serial Port (for differential capability)
Borland C++ compiler, Rev 3.1 or 4.0*

* to recompile the source code.

Note: We do not provide technical support of changes made to the product as supplied

GPS*Builder-2.1* kit contents

Single, half-size PCB
Active Antenna (gain: 26dB, NF <2.5dB) with SMA side-mounted connector. Magnetic mount
10 meters (33 feet) antenna cable with SMA connectors
Software on 3.5 inch HD diskette
Operating Manual with schematics, flow charts and tutorial, Software license agreement

Section 5
Application Notes

GEC PLESSEY
SEMICONDUCTORS

DW9255

SAW BANDPASS FILTER FOR GLOBAL POSITIONING SYSTEMS

(Supersedes version in February 1995 Microwave Products Handbook, HB3198-2)

GENERAL DESCRIPTION

The DW9255 is a SAW Bandpass filter operating at 35.42MHz with a passband width of 1.8MHz. The device is realised on a Lithium Tantalate substrate and housed in a leadless ceramic surface mount package.

The filter is customised for operation with the GEC Plessey Semiconductor Global Positioning Receiver chip set.

Competitive technologies include lumped element LC filters which offer substantially reduced performance at the expense of increased size but reduced cost.

OPERATION

A block diagram of a typical Global Positioning Receiver architecture is shown in Fig 1. GPS receivers operate at 1575.2MHz using a spread spectrum signal with 1.023Mbps BPSK modulation. The signal at the antenna is about -130dBm so the wanted signal is actually below the noise level.

The front end may consist of a low noise discrete transistor amplifier sandwiched by two high Q ceramic filters. The signal is then downconverted within the GP2010 chip using an internally synthesised 1400MHz local oscillator. The 1dB input compression point of -20dBm means that with subsequent filtering it is possible to reject large out of band jamming or interference signals. The output of this first stage downconversion is at 175.42MHz. In avionic or military applications where potential interfering signals may be in close proximity e.g. Inmarsat transmitters, it is recommended that a SAW filter be used to provide the pre-requisite levels of immunity to interference. In civil and commercial applications simple LC filtering should be adequate.

The second stage downconversion provides further gain and mixes down the signal using an internally generated 140MHz local oscillator to a second IF at 35.42MHz. At this point it is recommended that the GEC Plessey Semiconductor DW9255 SAW filter is used. The filter has a bandwidth of 1.8 MHz as required to pass the GPS data rate. The signal shaping features of the SAW filter at this second IF are a major determinant factor in the overall signal to noise figure of the system. Use of an LC filter in this application will degrade the S/N figure by over 3dB. The probable implication of this degradation is most apparent in reduced acquisition in urban areas of application and increased acquisition time in maritime applications.

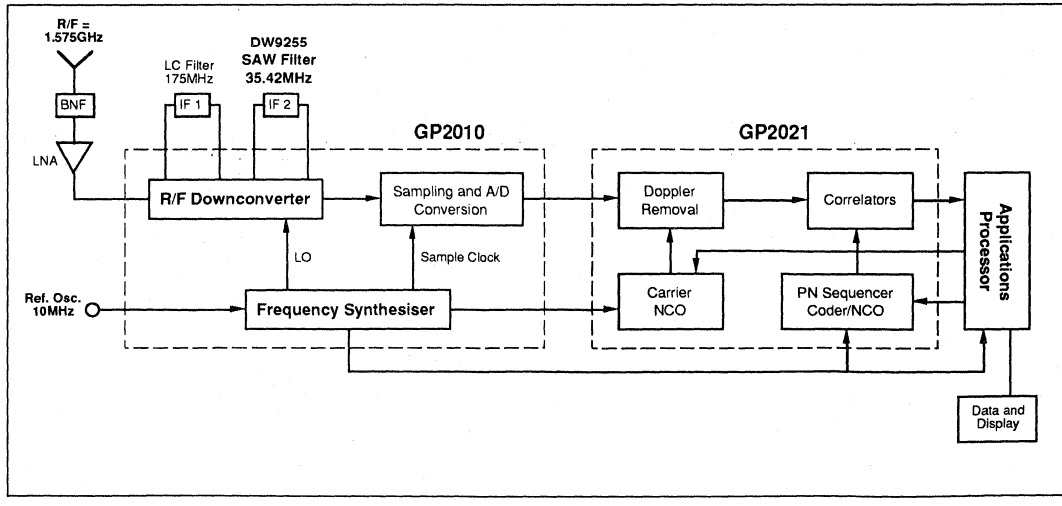


Figure 1: Block Diagram

Furthermore, the filter provides rapid roll-off to suppress unwanted adjacent channel interference. This interference problem becomes all the more apparent when the signal undergoes a third downconversion using a 31.1MHz local oscillator to 4.31MHz. Although some on chip LC filtering is provided within the GP2010 chip, filtering from the DW9255 SAW filter is essential to suppress in particular, spurii from the sampling clock at 5.71MHz, only 1.4MHz off the centre frequency. The DW9255 SAW filter provides over 10dB rejection to this potential source of interference. It does this in a very compact space needing only single element chip inductors shunted across the input and output terminals. In addition the group delay ripple and the in-band ripple of the filter are maintained below 100ns and 0.5dB respectively. The tight control of these parameters is essential if the system Bit Error Rate (BER) and resolution is to be realised.

Simple compact LC lumped element filters can only be used in place of the DW9255 SAW filter at significant expense to the overall system performance. In particular it is deemed unsuitable for urban transportation and marine applications, where triangulation may not be achievable due to the inability to locate the requisite number of satellites.

SAW FILTER DESIGN

Lithium tantalate is chosen as the piezoelectric SAW substrate because of its significantly better temperature stability over Lithium Niobate. More importantly, a "transversal" filter structure is used in preference to a "resonator" due to the simplicity of the matching networks and the option to drive the device in a balanced or unbalanced mode. Furthermore the group delay ripple in transversal filters is an order of magnitude better than equivalent resonator filters. This is particularly important in most digital communications systems as phase distortion is commonly the limiting factor in many designs. The enhanced phase ripple performance is at the expense of an increased insertion loss, typically 16dB. This has little to no effect on the system noise figure being buffered in the second IF. The impedance of the SAW device is designed to permit a simple single element inductive matching network on both the input and output to the device.

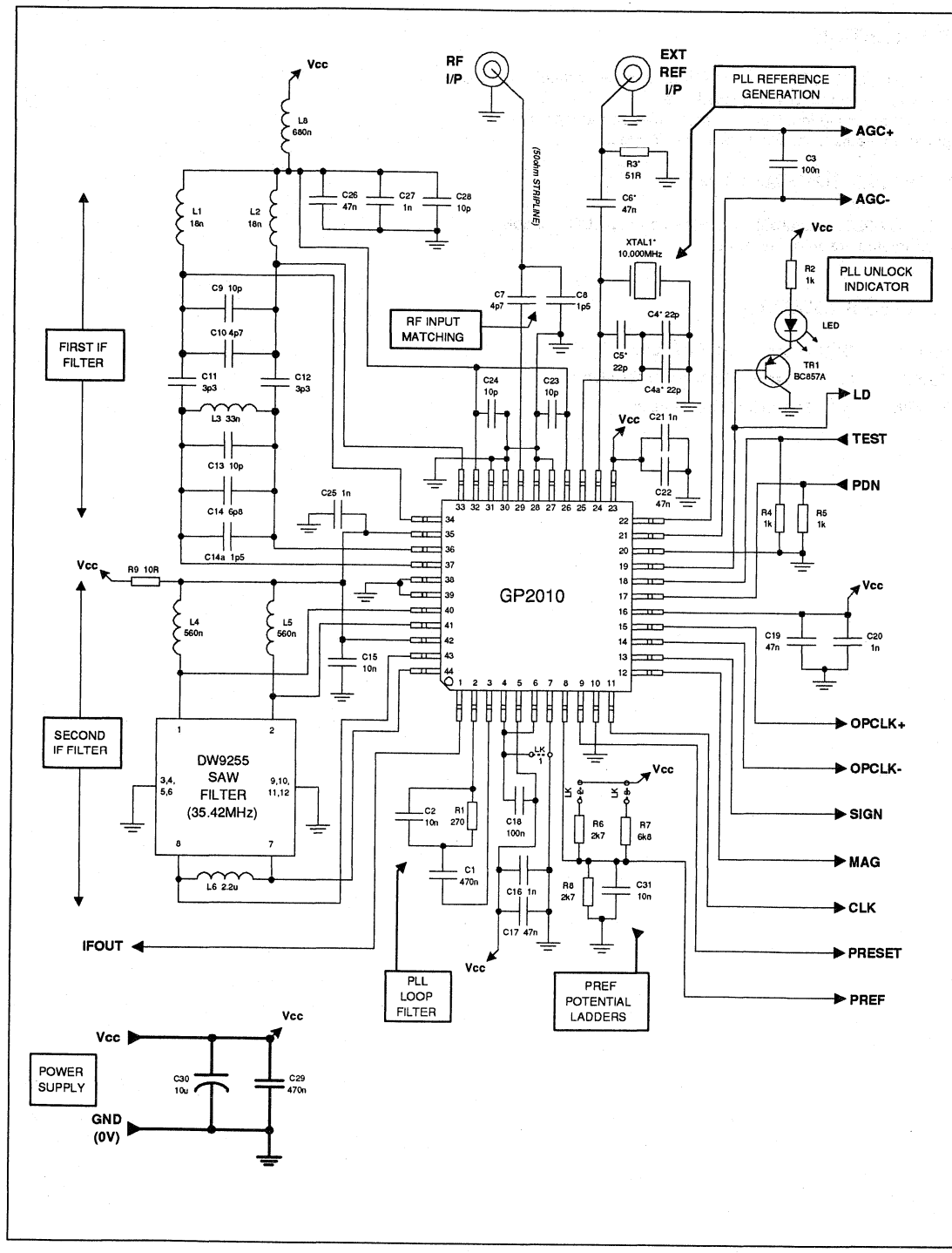


Figure 2: Evaluation Board Circuit

INSTALLATION

The DW9255 SAW filter is supplied in a hermetically sealed, surface mount ceramic package.

Shunt matching inductors are recommended to match the input and outputs to the SAW as shown in Fig 2.

ORDERING INFORMATION

The DW9255 is available in a SMT ceramic LCC, suitable for automated assembly systems.

RELATED PRODUCTS

GP2010	GPS Receiver - RF Front End
GP2021	GPS Receiver - 12 channel correlator
P60 ARM	ARM 60 RISC Microprocessor

GP2010

DESIGN WITH THE GP2010

(This Application Note should be used in conjunction with the GP2010 Datasheet, DS4056)

The GP2010 is a complete RF front-end for the Global Positioning System (GPS). A complete GPS receiver can be constructed with the addition of an active antenna with low noise amplifier (LNA), a GPS correlator IC (GP2021), a microprocessor and associated memory. A block diagram of a typical application circuit for the GP2010 appears in figure 1.

The GP2010 device converts the direct-sequence spread-spectrum signal in the L1 band (1575.42MHz) from a GPS antenna via a low-noise amplifier to a final IF at 4.309MHz, which is then digitised into a 2-bit data-stream. An on-chip phase-locked loop (PLL) is used to provide the local-oscillator frequencies to the mixers, which can be locked to a 10.000MHz reference signal from a variety of sources. A temperature controlled crystal oscillator (TCXO) is a preferred reference frequency source, allowing superior GPS signal tracking.

The GP2010 has been designed to operate with an active antenna with a gain of *greater* than +15dB (at 1575.42MHz).

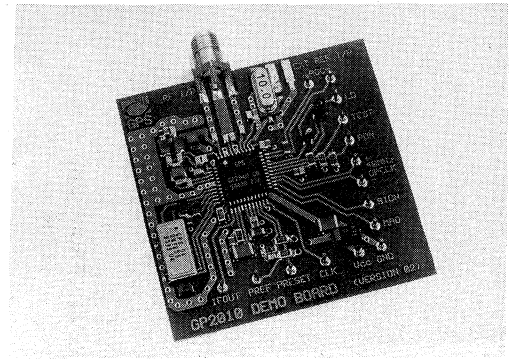
A detailed description of the GP2010 Integrated Circuit is given in the GP2010 data-sheet (No. DS4056).

DEMONSTRATION BOARD

The performance of the GP2010 GPS RF Front-end can be evaluated using the GP2010 Demonstration Board (available from GEC Plessey Semiconductors). The 44 pin GP2010 and ancillary components are mounted on a double-sided printed circuit board (PCB), allowing easy down-conversion of the GPS Coarse-Acquisition (C/A) coded signal from L1.

The GP2010 Demonstration Board consists of:-

- The GP2010 GPS front-end integrated circuit
- IF bandpass filters centred at 175.42MHz (coupled tuned LC) and 35.42MHz (SAW)
- PLL 10.000MHz reference crystal and loading
- PLL loop filter (15kHz bandwidth)
- PLL unlock indicator LED
- Vcc level sensing potential ladders for Power-on Reset
- AGC filter components
- RF Input matching components (matched to 50Ω)
- Power supply decoupling components



GP2010 Demonstration Board

The supplied 10.000MHz crystal can be removed from the board and a co-axial socket added for connection of an externally generated PLL reference. (See the section "Using an external PLL 10.000MHz reference frequency section" for details).

NOTE:- there is no facility on the board for RF Input filtering, or DC feed to an Active Antenna.

A circuit diagram of the GP2010 Demonstration Board appears in fig.2, and the layout of the PCB appears in fig.3.

Although there is no digital circuitry associated with the GP2010 on this Demonstration Board, the layout for the board can be implemented in any GPS receiver design, with no degradation in RF performance.

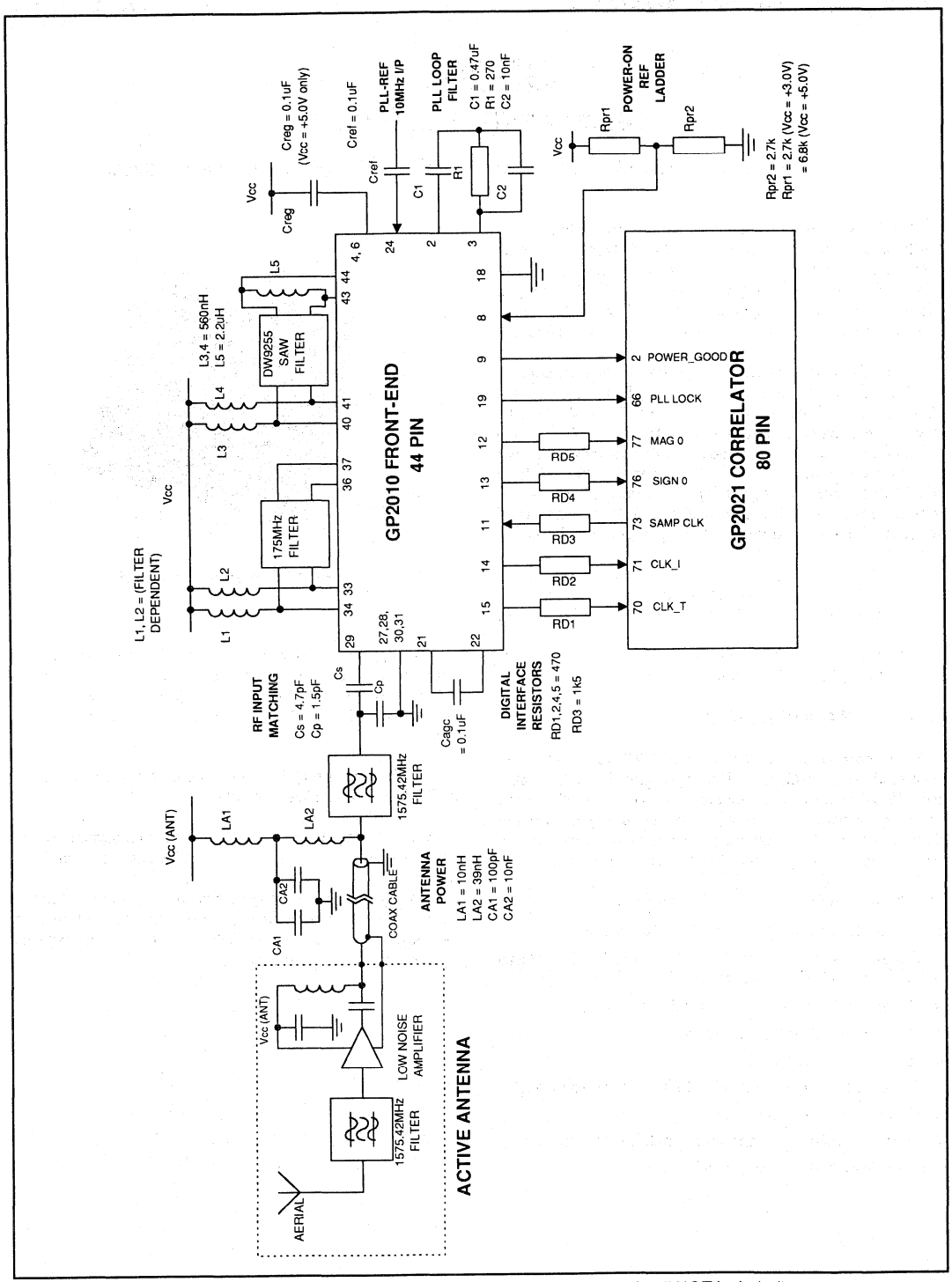
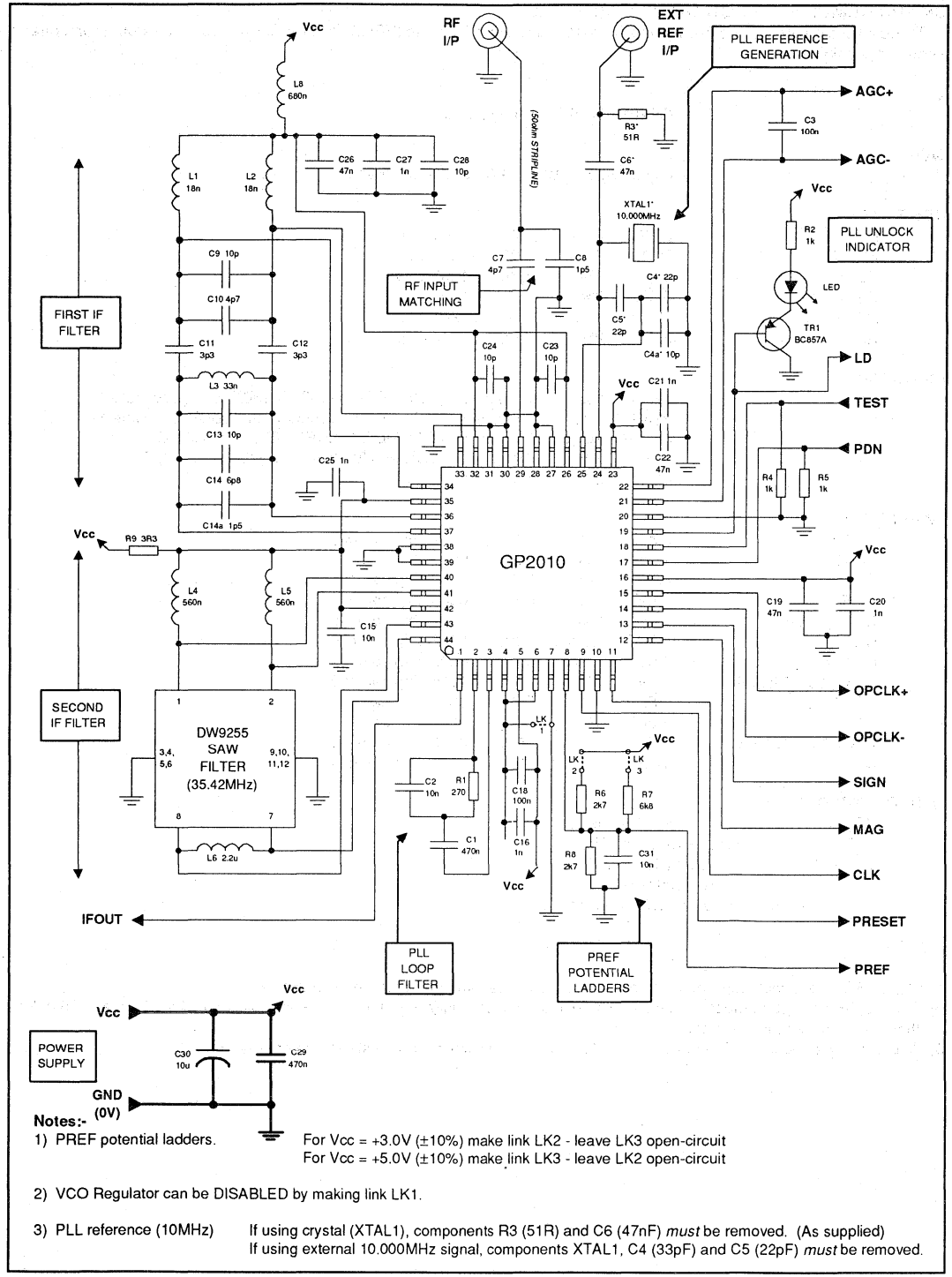


Fig.1 Typical GPS receiver RF application circuit (correlator detail NOT included)



Notes:-

1) PREF potential ladders. For Vcc = +3.0V (±10%) make link LK2 - leave LK3 open-circuit
For Vcc = +5.0V (±10%) make link LK3 - leave LK2 open-circuit

2) VCO Regulator can be DISABLED by making link LK1.

3) PLL reference (10MHz) If using crystal (XTAL1), components R3 (51R) and C6 (47nF) *must* be removed. (As supplied)
If using external 10.000MHz signal, components XTAL1, C4 (33pF) and C5 (22pF) *must* be removed.

Fig.2 Demonstration Board Circuit diagram

GP2010 DEMONSTRATION BOARD PARTS LIST

The following list of parts are used on the GP2010 Demonstration Board (VERSION 2), which uses surface mount components wherever possible:-

IC

GP2010 GPS Front-end device

SAW

DW9255 35.42MHz SAW - 2MHz passband

RESISTORS

R1	270Ω	2%,	1/4W,	1206 chip
R2,4,5	1kΩ	2%,	1/4W,	1206 chip
R3	51Ω	2%,	1/4W,	1206 chip
R6,8	2k7Ω	2%,	1/4W,	1206 chip
R7	6k8Ω	2%,	1/4W,	1206 chip
R9	3R3	2%,	1/4W,	1206 chip

INDUCTORS

L1, 2	18nH	5%,	1008 chip	(COILCRAFT 1008CS-180XJBC) (See Note 1)
L3	33nH	5%,	1008 chip	(COILCRAFT 1008CS-330XJBC) (See Note 1)
L4, 5	560nH	10%,	0805 chip	(TDK MLF2012DR56KT) (See Note 2)
L6	2u2H	10%,	0805 chip	(TDK MLF2012A2R2KT) (See Note 2)
L8	680nH	20%,	1008 chip	

CAPACITORS

C1,29	0.47uF	10%,	16V,	1812 chip ceramic
C2,15	10nF	5%,	50V,	0805 chip ceramic
C3,18	0.1uF	10%,	16V,	1206 chip ceramic
C4,5	22pF	5%,	50V,	0805 chip ceramic
C6,19,22,26	47nF	5%,	50V,	0805 chip ceramic
C7,10	4.7pF	±1/4pF,	50V,	0805 chip ceramic
C8,14a	1.5pF	±1/4pF,	50V,	0805 chip ceramic
C4a,9,13,23,24,28	10pF	5%,	50V,	0805 chip ceramic
C11,12	3.3pF	±1/4pF,	50V,	0805 chip ceramic
C14	6.8pF	±1/4pF,	50V,	0805 chip ceramic
C16,20,21,25,27,31	1nF	5%,	50V,	0805 chip ceramic
C30	10uF	20%,	16V,	2412 chip tantalum

OTHER COMPONENTS

XTAL1		10.000MHz Crystal
LED1		Red LED - high efficiency
TR1		BC857A PNP transistor
	2 off	SMA panel jack
	19 off	Veropins 1.02mm diameter

NOTES:-

1) COILCRAFT or similar high performance inductors are recommended for the first IF filter
2) SCREENED inductors must be used for the second IF filter. Digital interference is easily picked up by L4, L5 and L6 unless they are magnetically screened.
3) ALL ceramic capacitors should use NPO, COG or X7R dielectric for high stability over temperature

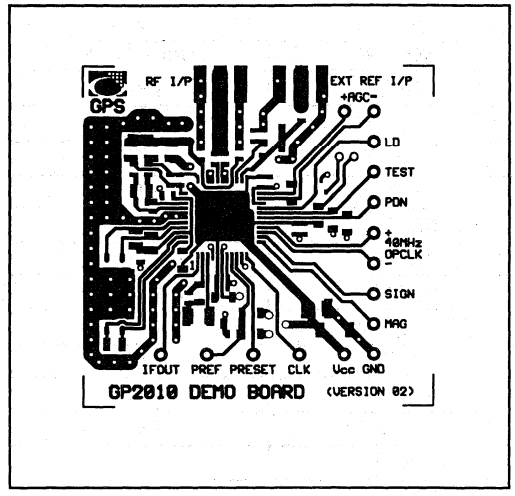


Fig.3a Layout Demonstration Board - upper copper layer (SCALE 1:1)

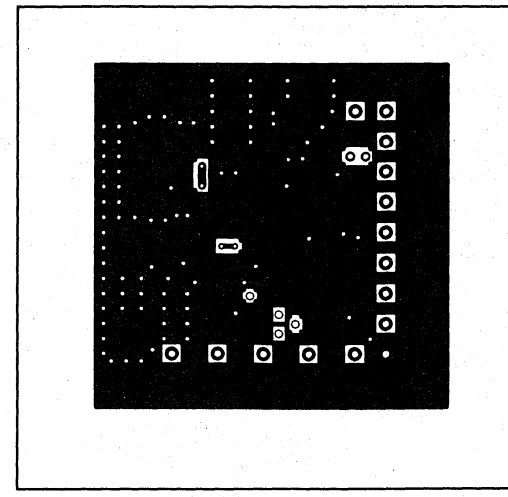


Fig.3b Layout Demonstration Board - lower copper layer (SCALE 1:1)

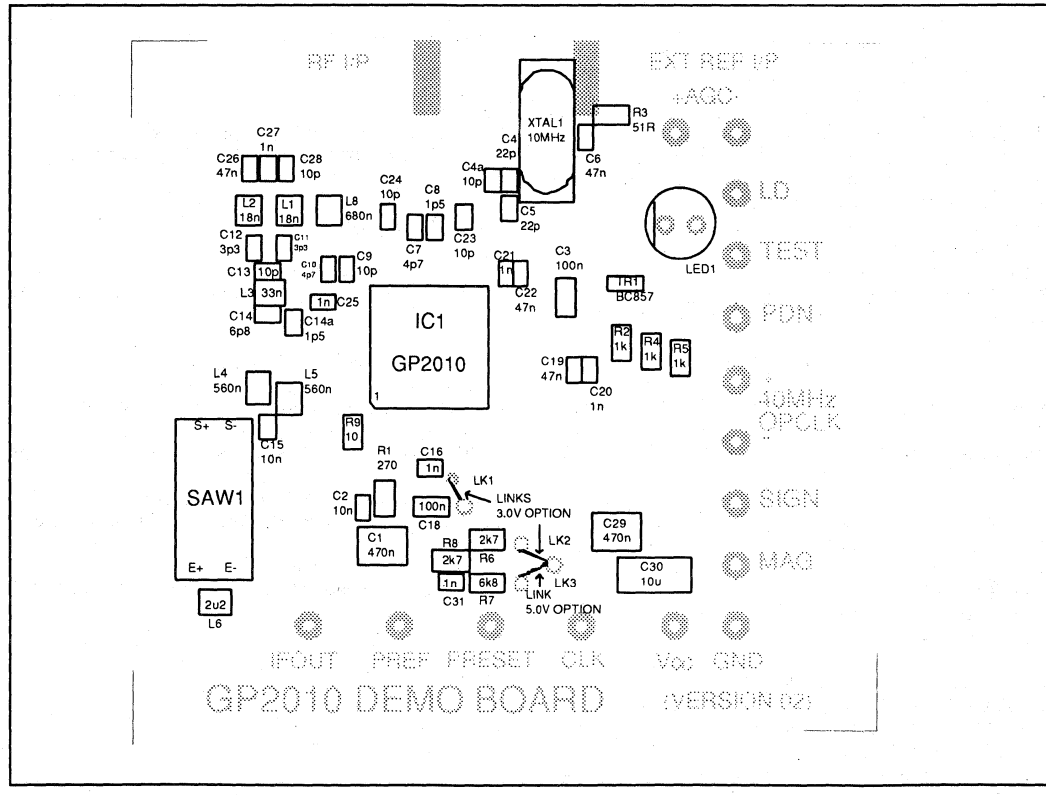


Fig.3c Layout Demonstration Board - component positions (SCALE 2:1)

OPERATING NOTES

The GP2010 Demonstration Board is provided with the following I/O connections:-

NAME	DESCRIPTION	I/O TYPE	CONNECTION
GND	0v supply	INPUT	PIN
Vcc	+ve supply	INPUT	PIN
CLK	Sample Clock input (5.71MHz)	INPUT	PIN
PRESET	Vcc level sense output	OUTPUT	PIN
PREF	Vcc level sense input	MONITOR/INPUT	PIN
IFOUT	IFOUT test point	OUTPUT	PIN
MAG	Magnitude bit digital output	OUTPUT	PIN
SIGN	Polarity bit digital output	OUTPUT	PIN
40MHz OPCLK+	40MHz clock positive output	OUTPUT	PIN
40MHz OPCLK-	40MHz clock negative output	OUTPUT	PIN
PDN	Power-down activation input	INPUT	PIN
TEST	PLL de-activation input	INPUT	PIN
LD	PLL lock detect output	OUTPUT	PIN
AGC-	AGC control negative	MONITOR	PIN
AGC+	AGC control positive	MONITOR	PIN
RF INPUT	RF signal input at 1575.42MHz	INPUT	SMA

The GP2010 is designed for operation from either +5.0V (±10%) or +3.0V (±10%) power-supply, although intermediate supply voltages can be used with care.

VCO SUPPLY REGULATOR

The GP2010 has an on-chip voltage regulator to provide an improved power-supply-rejection-ratio (PSRR) to the VCO. The regulator provides a +3.3V supply to the VCO when used with supply voltages (Vcc) of greater than +4.0V. It is strongly recommended that the VCO regulator is used where possible, in order to improve spurious rejection in the VCO. An improvement of 25dB in the PSRR of the VCO can be achieved using the regulator, over the 100Hz to 1MHz frequency range.

If the supply voltage (Vcc) is less than +4.0V, the function of the VCO regulator cannot be guaranteed, and so it should be disabled (refer to GP2010 data-sheet, fig.7). This is achieved by connecting VEE(OSC) (pins 4 & 6) to VEE(REG) (pin 7) or 0V.

A link (LK1) on the demonstration board (see Note 2, in figure 2) allows VEE(OSC) (pin 6) to be shorted to 0V.

5.0V OPERATION

To operate the Demonstration Board from +5.0V, the following connections are needed:-

- 0V DC connection to GND INPUT pin
- +5.0V DC connection to Vcc INPUT pin
- 5.71MHz digital clock connection to CLK INPUT pin (CLK low <+0.5V, CLK high >+2.0V)
- RF signal at 1575.42MHz connected to RF INPUT SMA socket.
- Power-on Reset (PREF) potential ladder - R6 (2k7Ω) *connected to Vcc*, R7 (6k8Ω) disconnected (see Note 1, in figure 2)

3.0V OPERATION

To operate the board from +3.0V, the following connections are needed. They differ from those for +5.0V operation:-

- 0V DC connection to GND INPUT pin
- +3.0V DC connection to Vcc INPUT pin
- 5.71MHz digital clock connection to CLK INPUT pin (CLK low <0.5V, CLK high >2.0V)
- RF signal at 1575.42MHz connected to RF INPUT SMA socket.
- Power-on Reset (PREF) potential ladder - R6 (2k7Ω) *connected to Vcc*, R7 (6k8Ω) disconnected (see Note 1, in figure 2)
- VCO voltage regulator *must* be disabled - connect VEE(OSC) (pin 4 & 6) to 0V (see Note 2, in figure 2)

PLL TEST INPUT

The GP2010 is provided with a TEST input, which when set to logic high (>2.0V) will *unlock* the PLL, and the VCO will operate at its highest frequency.

In normal operation, the TEST input must be at logic low (<+0.5V), which can be achieved easily by connecting TEST to 0V directly or via a 1kΩ resistor.

POWER-UP AND POWER-ON RESET CIRCUIT

On power-up, the LED which is driven from the LD output line should blink ON once, then remain OFF, as the on-chip PLL locks to the 10.000MHz reference. Also, the power-on reset (PRESET) output should toggle from logic low (0V) to logic high (Vcc). PRESET will remain at logic high unless the supply voltage reduces significantly, causing the voltage applied to the PREF input to drop below +1.21V. If the supply voltage should reduce then the PRESET output will set to logic low, indicating a power-supply failure.

A potential divider for use with the PREF input (pin 8) is shown in fig.4.

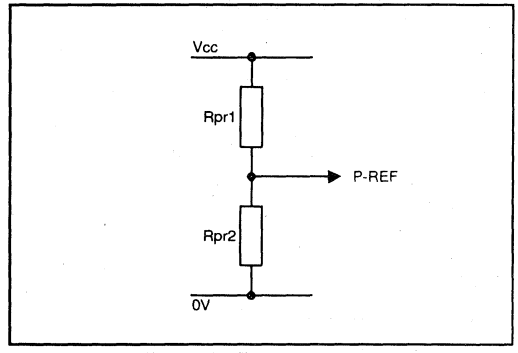


Fig.4 PREF potential divider

The value of supply voltage (Vcc(thresh)) at which the PRESET output toggles can be adjusted by changing the values of resistor in the PREF potential divider, as per the formula:-

$$Vcc(thresh) = \frac{1.21V \times (Rpr1+Rpr2)}{Rpr2}$$

The values used with the demonstration board (refer to fig.2) are:-

i) Vcc = +5.0V, LK3 made, LK2 open, Rpr1 = R7 = 6k8Ω & Rpr2 = R8 = 2k7Ω, giving Vcc(thresh) = +4.25V.

ii) Vcc = +3.0V, LK2 made, LK3 open, Rpr1 = R6 = 2k7Ω & Rpr2 = R8 = 2k7Ω, giving Vcc(thresh) = +2.42V.

The correct PLL frequency can be monitored from the OPCLK+ & OPCLK- output pins. The signal from these will be exactly 40MHz when the PLL is locked correctly (1400MHz divided by 35), at a level of approximately 100mV peak-to-peak. The two OPCLK pins give a balanced differential 40MHz output.

POWER DOWN (PDN) INPUT

The GP2010 is provided with a PDN input, which when set to logic high (>+2.0V) will power-down ALL the chip functions (except for the Power-on Reset function) resulting in a greatly reduced current consumption.

In normal operation, the PDN input must be at logic low (<+0.5V) which is easily achieved by connecting PDN to 0V directly or via a 1kΩ resistor.

ANALOG TO DIGITAL CONVERTER

By applying a digital clock to the CLK input pin, the sampled IF output will appear as a 2-bit quantised signal at the SIGN and MAG pins. The SIGN data indicates the *polarity* of the digital IF signal, and the MAG data indicates the *amplitude*. The data from the SIGN and MAG pins is in Not-Return-to-Zero (NRZ) format (hence the data is latched for the whole CLK period). The operation of the AGC in the 3rd IF stage is determined by a comparator (which operates independently of CLK) to give a MAG duty-cycle of 30% (nominal) over the AGC control range. The duty-cycle refers to the number of logic high states from MAG over a given number of CLK periods. Both MAG and SIGN data are latched on the *rising* edge of the CLK digital clock

The frequency of the sampling CLK input signal can be user-defined. When the GP2010 is used with the GP2021 correlator, the sampling frequency is 5.71MHz (40MHz divided by 7), which aliases the 4.309MHz analog IFOUT down to a 1.405MHz digital IF.

USING AN EXTERNAL PLL 10.000MHZ REFERENCE FREQUENCY

The GP2010 Demonstration Board is supplied with a 10.000MHz crystal as the PLL frequency reference, to allow easy evaluation of the GP2010. However, the frequency stability of a crystal may not be high enough for a complete GPS receiver, and a 10.000MHz temperature compensated crystal oscillator (TCXO) may be preferred. This can be easily achieved by removing the crystal and the loading capacitors (C4, C4a & C5) from the board and replacing them with a 10.000MHz frequency source (applied via a coax line to an SMA, or equivalent, connector which can be added to the board), a 50Ω termination, and a 47nF coupling capacitor to the REF 2 input (pin 24) - see Note 3, on fig.2.

The amplitude of the 10.000MHz frequency source *must* be > 0.1V and <1.2V peak-to-peak. If the amplitude is greater than 1.2V peak-to-peak, a spurious output may appear on the IFOUT signal (refer to section "Spurious signals in the IF spectrum"). In this case the signal should be attenuated.

A suitable 10.000MHz TCXO is the *Rakon TXO4080,* with a 1.0V peak-to-peak *minimum* clipped sinewave output amplitude. This TCXO can be connected to the GP2010 as shown in figure 5, with the addition of a 6dB attenuation of this signal to produce a 0.5V peak-to-peak amplitude - optimum for GP2010.

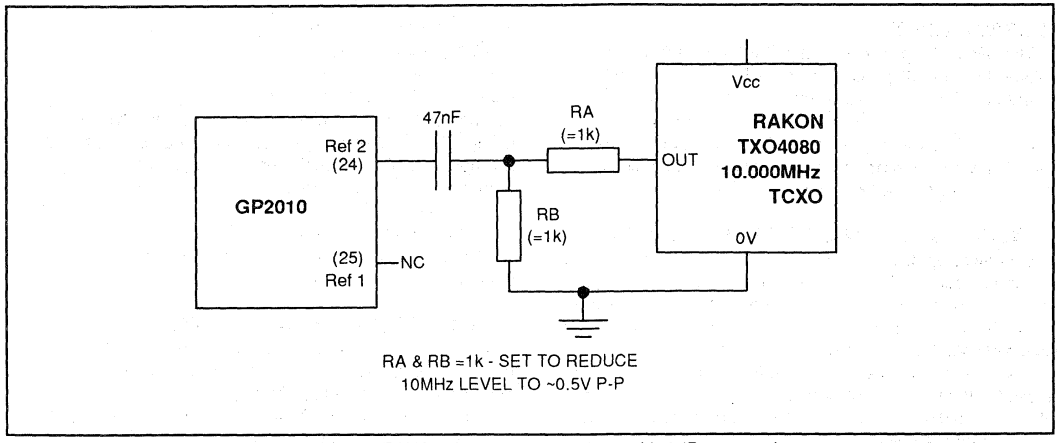


Fig.5 Rakon TCXO reference connections with 6dB attenuation

PLL LOOP FILTER AND VCO PERFORMANCE

The GP2010 has an on-chip PLL to produce all the local-oscillator frequencies for the IF mixers. The recommended PLL loop filter produces a third-order PLL with a second-order external filter comprising 2 capacitors and 1 resistor, as shown in fig.6.

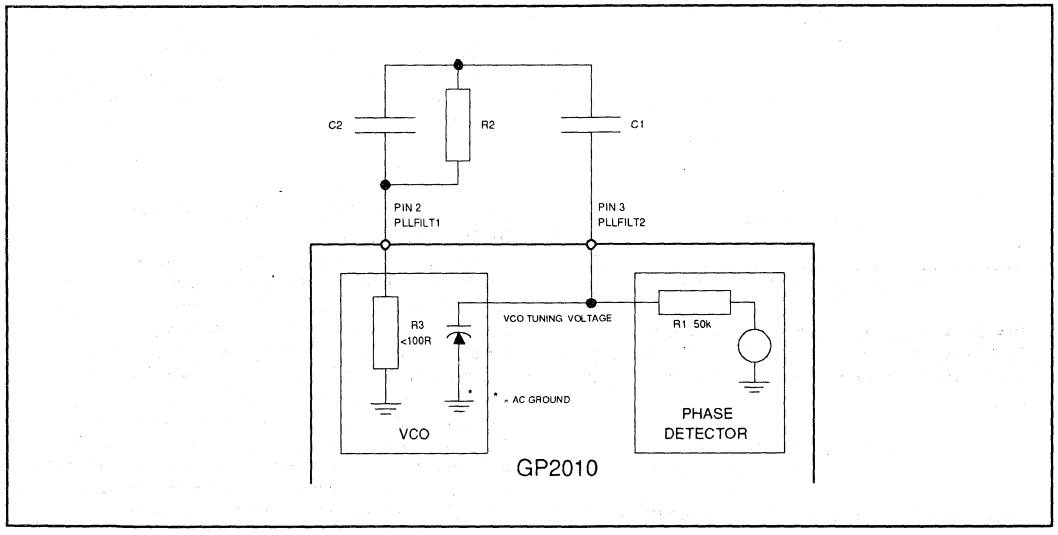


Fig.6 PLL loop filter showing relevant on-chip components

The loop filter is used to roll off the response of the PLL at high frequency, but maintain loop stability at the loop-bandwidth frequency (where loop gain = 1 (0dB)). The optimum values for this PLL loop filter can be calculated knowing the loop-gain, phase-margin and required loop bandwidth.

The loop gain at 1radian/second can be calculated as a ratio (NOT dBs) as follows:-

$$\text{Loop Gain } (G_L) = \frac{K_D K_V}{N}$$

where :- K_D = Phase detector gain
K_V = VCO gain
N = Loop division ratio (140)

G_L is between 3.1×10^6 and 100×10^6 for the GP2010 (130dB and 160dB).

Knowing the loop gain, the time-constants of the filter can be calculated as follows:-

$$\tau_1 = \frac{G_L}{\omega_n^2}\sqrt{\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}} \quad \text{..... (1)}$$

$$\tau_2 = \frac{1}{\omega_n^2\tau_3^2} \quad \text{..... (2)}$$

$$\tau_3 = \frac{-\tan\phi + \frac{1}{\cos\phi}}{\omega_n} \quad \text{..... (3)}$$

where:- G_L = PLL loop gain at 1radian/second offset
τ_1 = time constant of first filter pole
τ_2 = time constant of filter zero
τ_3 = time constant of second filter pole
ω_n = PLL loop bandwidth
ϕ = PLL phase margin

For the PLL loop filter referred in fig.6:-

τ_1 = R1C1
τ_2 = R2(C1+C2)
τ_3 = R2C2

Resistor R3 (on-chip) can be regarded as an AC ground since its value is much smaller than R1 (50kΩ).

The recommended PLL loop filter has the following values for external components, giving a nominal loop-bandwidth of 15kHz and phase-margin of 60°:-

C1 = 470nF
R2 = 270Ω
C2 = 10nF

The higher the phase margin (ϕ) of the loop filter at the loop bandwidth (ω_n), the higher the stability of the PLL across the full range of loop gain. The graph in fig.7 shows the loop filter response for the loop-filter components defined above, and fig.8 shows the spectrum of the 1400MHz VCO signal from a GP2010 at +25°C, with the VCO regulator enabled.

There are further components on chip which produce bandwidth limiting within the phase-detector. These provide two further poles in the PLL filter response at 400kHz (2.51Mrads/sec) and 530kHz (3.33Mrads/sec). These have negligible effect on PLL loop stability provided the PLL loop bandwidth is less than 100kHz.

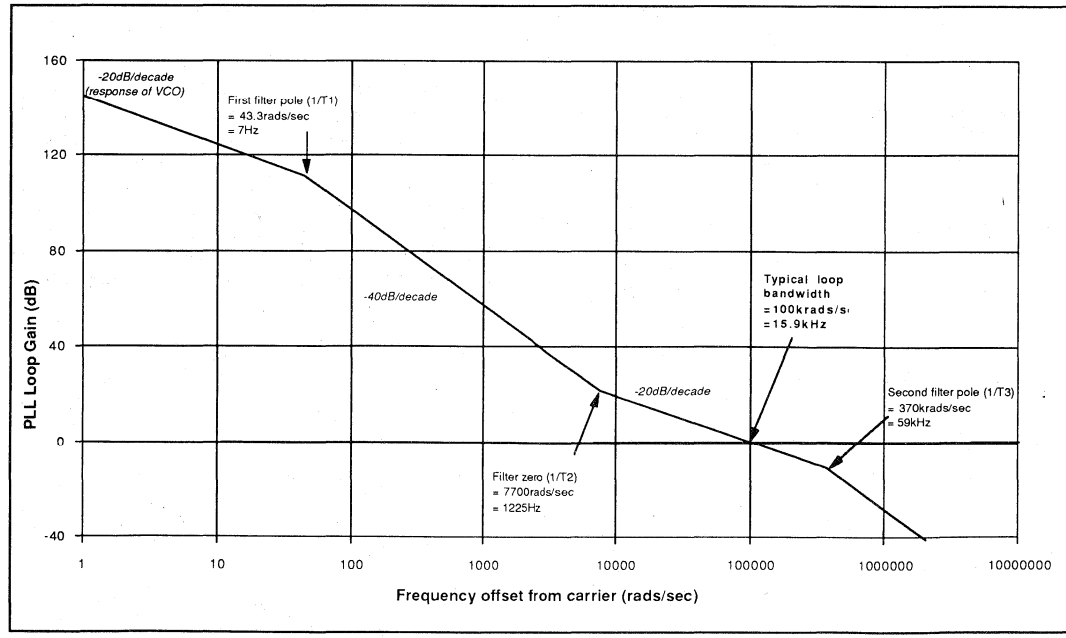


Fig.7 Typical GP2010 PLL loop gain (G_L) vs. frequency

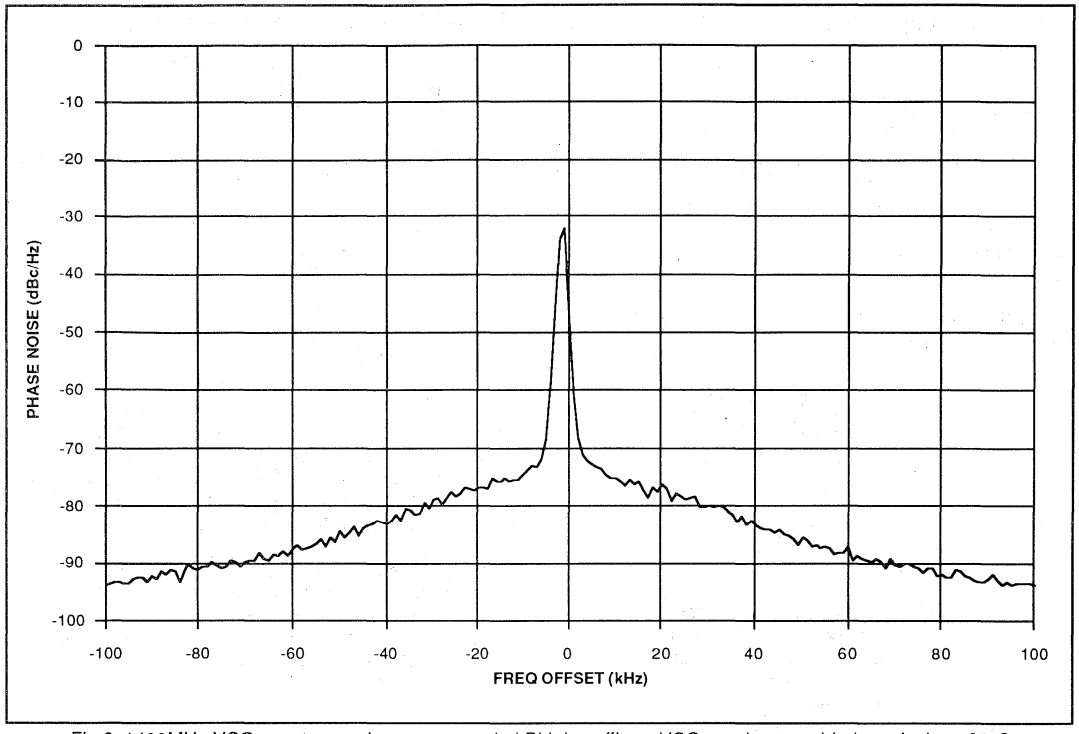


Fig.8 1400MHz VCO spectrum using recommended PLL loop filter - VCO regulator enabled - typical at +25°C

IFOUT SPECTRUM

The IFOUT output is a high impedance (1kΩ) monitor point, for test purposes only, which can be used to monitor the output of the IF chain before the analog-to-digital converter. Figs 9, 10 & 11 show typical IFOUT spectra for the GP2010, under differing operating conditions:-

Fig.9:- NO RF INPUT signal, NO 5.71MHz digital clock applied to CLK;

Fig.10:- NO RF INPUT signal applied, a 5.71MHz TTL clock applied to CLK via 1kΩ series resistor;

Fig.11:- RF INPUT signal applied from a GPS antenna with 26dB Gain and 2.5dB noise figure and a 5.71MHz TTL clock applied to CLK via 1kΩ series resistor;

Observe that the on-chip AGC suppresses the level of out-of-band noise and spurious signals as the level of noise at 1575.42MHz at the RF input increases (the GPS signal is buried in noise). The spectrum in fig.11 is typical of that produced by a working GPS receiver using the GP2010.

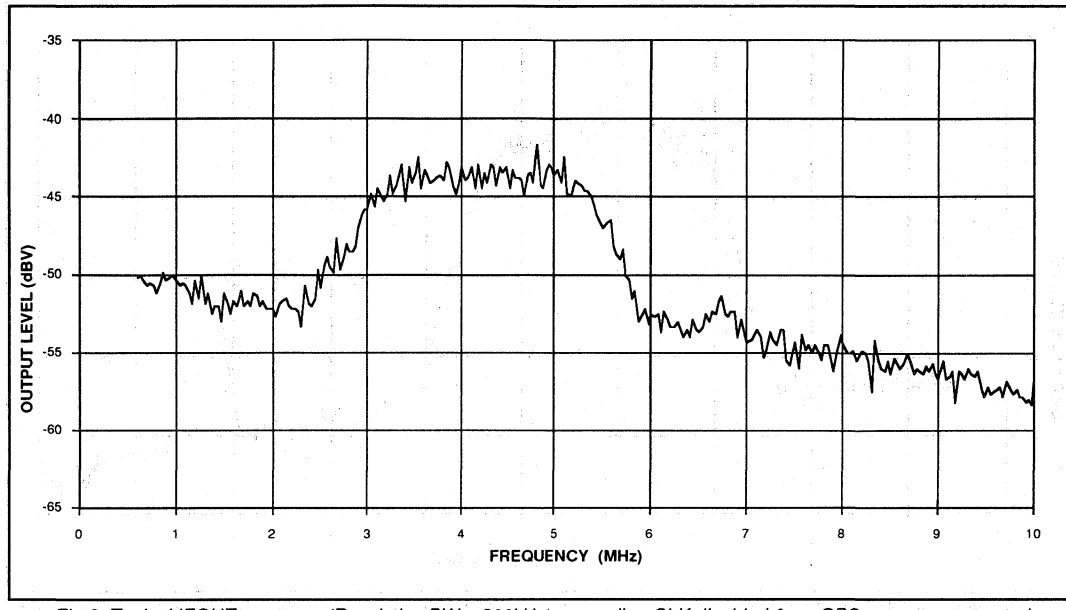


Fig.9 Typical IFOUT spectrum (Resolution BW = 300kHz) - sampling CLK disabled & no GPS antenna connected

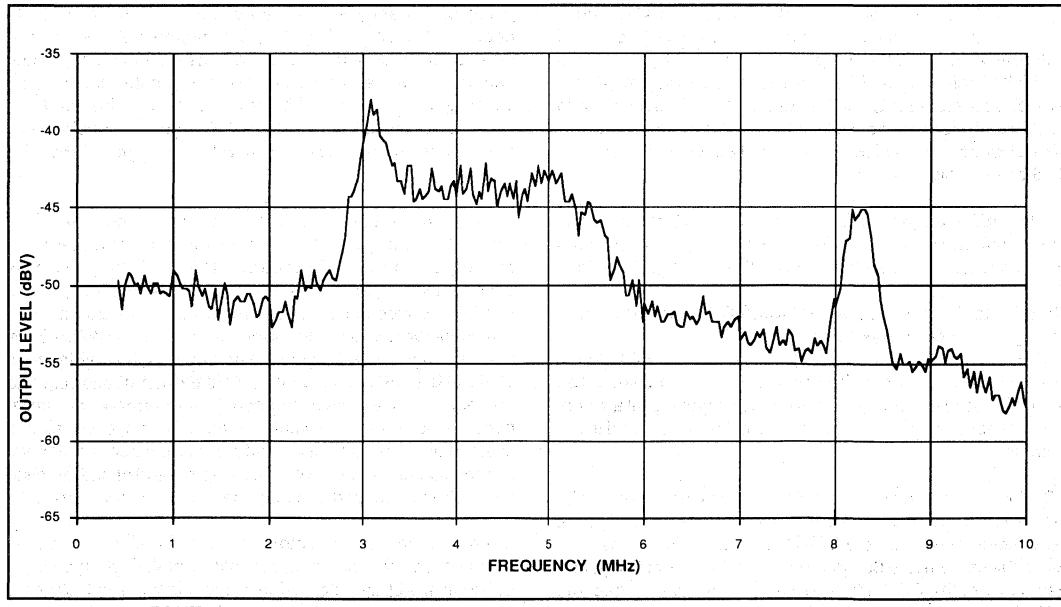


Fig.10 Typical IFOUT spectrum (Resolution BW = 300kHz) - 5.71MHz sampling CLK enabled & no GPS antenna connected

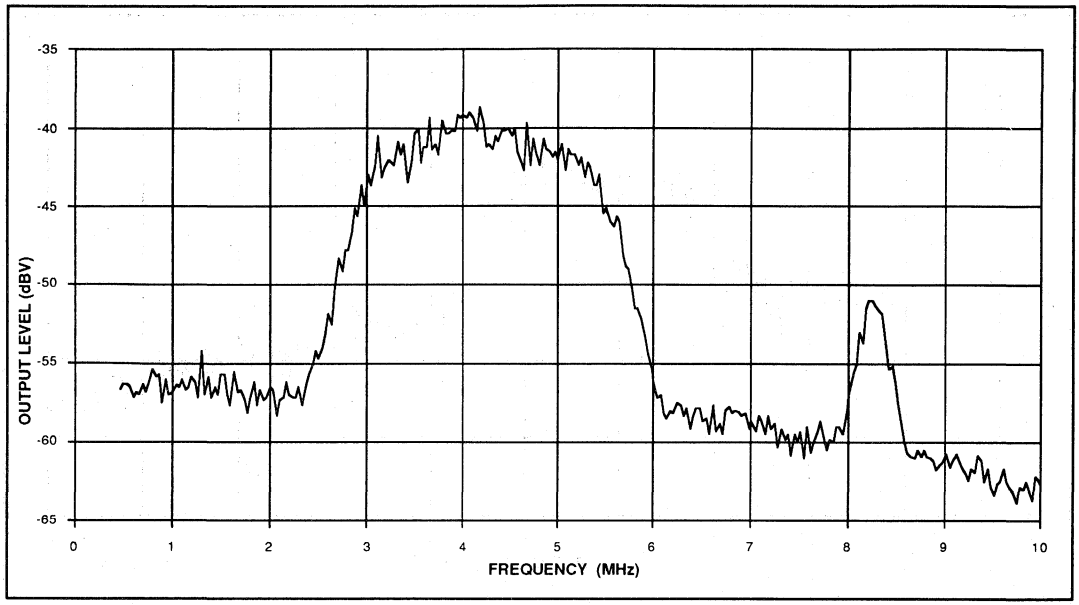


Fig.11 Typical IFOUT spectrum (Resolution BW = 300kHz) - 5.71MHz sampling CLK enabled & GPS antenna connected

SPURIOUS SIGNALS IN THE IF SPECTRUM

For the GP2010 to work correctly, the stage 3 AGC circuit should set the level of noise in the mixed-down GPS L1 band (4.309MHz ±1.023MHz) to approx 100mV r.m.s (nominal) at the IFOUT (pin 1). Any IF spurs should be suppressed to a level of *less* than -20dBc of the nominal IFOUT level to avoid the AGC attenuating the noise in the band of the mixed-down GPS L1 signal to a level which the correlator will cease to track GPS satellite signals.

The GP2010 uses a balanced-signal architecture, and is largely immune to spurious signals. However, there are some exceptions (refer to spectral plots of IFOUT in figs 10 & 11):-

Digital interference spurs, including CLK sampling the analog to digital converter.

Some digital signals can couple across the GP2010 chip independently of any peripheral components. Care should be taken to ensure that harmonics of the CLK input signal are kept to a minimum so that they do not become mixed in-band in the IF chain.

If CLK is at a frequency of 5.71MHz (typical application with GP2021), spurious signals *can* appear on the IFOUT pin at frequencies of 8.25MHz, 2.54MHz and 3.17MHz. These are due to the 4th, 5th and 6th harmonics of CLK respectively, and they can jam the AGC if they are large, and hence affect the GPS data from the MAG and SIGN outputs.

Harmonics due to CLK can be reduced by attenuating the CLK signal input to the GP2010 to a 2V amplitude using a potential divider (typical resistor values in the region of 1kΩ - dependent upon level of Vcc). An alternative method is to insert a 1k5Ω resistor in *series* with the CLK input, the upper harmonics can be rolled off by creating a pole with the input capacitance. Care should be taken to ensure that the MAG and SIGN output latches on the GP2010 do not "double-clock" (i.e. trigger on both the rising *and* falling edges of the CLK signal).

Jamming interference can also occur from the close proximity of the GP2010 to associated microprocessor and memory circuitry in a GPS receiver. This is primarily due to the sensitivity of the 3rd stage mixer with a high-value inductor used to produce the bandpass response in the 2nd IF filter. The inductor (L6) used to resonate with the DW9255 SAW filter is a high value (2.2μH) which has a high impedance at 35.42MHz (~490Ω), which has a side-effect of allowing it to operate as an effective antenna to interference at similar frequencies. L6 is particulary vulnerable to pickup as it is situated after the SAW filter, and signals injected at that point are not rejected by the SAW. The amplitude of digital jamming spurs can be reduced by using the following techniques:-

a) L4, L5 and L6 inductors around SAW filter can be magnetically - screened, monolithic multi-layer types.
b) Mount the L6 inductor inside a screening can, but take care to ensure that the self-resonant frequency and inductor Q are *not* greatly reduced.
c) Mount the L6 inductor coil in an *orthogonal* plane (vertical) to the digital tracks on the PCB.

d) Ensure that *no* power-supply and digital tracks run in close-proximity to the L6 inductor. Ideally the L6 inductor should be surrounded by ground-plane on *all* board layers for a radius of >15mm.

In practice, in all but the most extreme environments, most benefits are obtained by using screened inductors, especially for L6, and by routing power and digital tracks clear of L6.

External 10.000MHZ PLL reference

Care should be used to ensure that the 10.000MHz PLL reference signal is AC coupled into the GP2010, and that the amplitude does not exceed 1.2V peak-to-peak. If the amplitude is higher than this, harmonics of the PLL reference can interfere with the 3rd stage mixer and produce interference spurs on the signal at IFOUT (in particular the third harmonic (30MHz) will produce a spur at 1.111MHz). A suitable attenuator should be used if a TCXO with TTL level outputs is used (refer to fig.5).

Self generated spurious signals

A spurious signal at 15.55MHz exists at the IFOUT resulting from an on-chip interaction between the second and third IF stages. The spur has variable amplitude but is always sufficiently low to have no effect on the 3rd IF stage AGC, or GPS signal reception.

ANTENNA DETAILS

The GP2010 has been designed to use the signal from a GPS antenna with a low-noise-amplifier (LNA). The noise figure of the complete receiver will then be dominated by the noise figure of the LNA. However, care should be taken to ensure that the gain of the LNA is high enough to allow the GP2010 to function correctly in a GPS receiver.

The GPS signal is spread-spectrum modulated with a 2.046 MHz bandwidth, and received power is in the region of -130dBm. The power of background noise in the same bandwidth is -111dBm, so the GPS signal is buried within the background noise. The GP2010 AGC operates on the noise in the band of the GPS signal and not on the GPS signal itself. The de-spreading of the GPS signal restores a positive signal-to-noise ratio. This is carried out by a DSP correlator chip - the GP2021 is recommended.

The power of the noise over a 2MHz bandwidth is 63dB up on the noise in a 1Hz bandwidth (-174dBm/Hz), giving a minimum signal power of approximately -111dBm. Consider also the following values (with reference to the "IF filter details" section and the Electrical Characteristics table in the GP2010 Data-sheet):-

Max IF gain of GP2010 (minimum guaranteed) =106dB ...(a)
Max attenuation of external IF filters = 21dB ...(b)
Nom IFOUT level with AGC operating (Stage 3) =100mV rms ...(c)

Notes:-

a) The maximum IF gain taking account of the loading effects of the IF filtering (but excluding filter losses)

b) The attenuation is the sum of the losses in 1st and 2nd IF filters

c) 100mV rms is equivalent to -7dBm in a 50Ω load

When the background noise within a 2MHz bandwidth is applied *directly* to the GP2010 RF input (with no LNA or RF Input filter) and all IF filters included (with DW9255 SAW - Loss typ. -17dB), the minimum signal produced at the IFOUT will be:-

-111+106-21 = **-26dBm**

For the AGC of 3rd IF stage to operate correctly on the applied signal, the signal level at IFOUT should be at -7dBm. This gives a shortfall in signal level of 19dB.

If a Low Loss 2nd IF filter is used in place of the DW9255 SAW, the minimum signal at the IFOUT will be greater than -26dBm, but will never be great enough to exclude the need for a LNA.

So an RF LNA with combined RF filter needs to provide at least 19dB more noise than would be provided by a passive antenna alone. The GPS receiver noise figure ideally needs to be kept low. Since the noise figure of the LNA will dominate the noise performance of the receiver, it is wise to use a LNA with N.F. of <3.0dB, which results in a *minimum* required LNA gain (plus RF filter loss) of **>+16.0dB.**

It is recommended that the LNA gain be kept to below 60dB, so as NOT to overload the GP2010.

Active GPS antennas can be of either patch or helical type. A recommended active GPS patch antenna is available from *M/A COM*-type *ANP-C-114*, which has an LNA gain of +26dB and a noise figure of ~2.5dB. If an RF filter (loss ~ -2.0dB) is connected between the antenna output and the RF Input to the GP2010, the resultant noise contribution of the LNA and filter will be in the region of **+26.5dB** - optimum for the GP2010.

(Note that the M/A-COM antenna above includes an 1575MHz ceramic resonator RF filter preceding that LNA.

IF FILTER DETAILS

The GP2010 has a triple conversion architecture. All three stages can be treated as separate blocks. User-defined filter networks can be used for IF filtering between stage 1 & 2, and between stage 2 & 3.

RF filter

The Stage 1 mixer has an on-chip image-rejection filter, with optimum pass band set at 1575.42MHz, and a rejection of the image frequency (1400-175.42MHz =1224.58MHz) of approximately 7dB. Image rejection is not critical at 1224.58MHz because this frequency is at approximately the GPS L2 frequency (1227.6MHz). So there is only noise at this frequency.

The Image filter is fixed, but can be enhanced by the addition of an external RF filter between the LNA and GP2010.

Centre Frequency	1575.42MHz
Pass Band	±1.0MHz minimum (within ±1.0dB)
RF Image frequency	1224.58MHz
Input Impedance	50Ω typical
Output Impedance	50Ω typical
Insertion loss	0.5dB -> 2.0dB

The RF filter is required to remove the 1224.58MHz image noise and to prevent overload of the Stage 1 mixer by strong out-of-band interference signals. The required performance of this filter will be influenced by any locally generated interfering signals that may be present (for example, mobile telephone). Ideally, the filter should reject any out-of-band interference to a level, at the GP2010 RF input, of at least 10dB below the level at which the Stage 1 mixer will gain compress by 1dB (refer to GP2010 data-sheet for 1dB compression level). The pass-band of this filter should be flat across the 2MHz bandwidth of the GPS C/A code signal. For most filter technologies the bandwidth will be significantly greater than this.

When specifying the RF filter, it is important to consider the filtering effect of the GPS antenna and low-noise amplifier. The majority of GPS antennas are patch types, which have a narrow bandwidth and will therefore provide some filtering. This can reduce the requirements of the RF filter used, and hence the cost of the overall receiver.

The insertion loss of the RF filter can affect the noise figure of the GP2010. The low-noise pre-amplifier which boosts the signal from the antenna to the GP2010 should be designed so that there is sufficient gain for the RF filter loss to have a negligible effect on overall noise figure.

A typical RF filter will be a dielectric type. Suitable filters are available from a range of manufacturers. A recommended type of RF filter is the *Murata DFC2 1R57 P002 BHD* which is centred on 1575.42MHz and has a 2MHz passband (-3.0dB).

The GP2010 requires components to match the input impedance to that of the RF filter output. Most filters have a 50Ω output impedance. Fig.12 shows the recommended matching circuit.

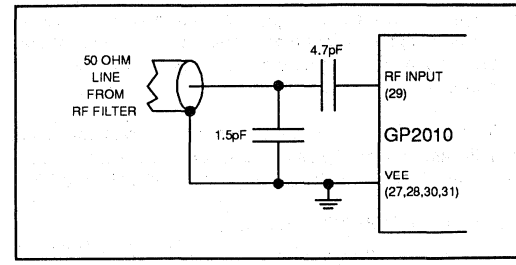


Fig.12 RF Input matching circuit

1st IF filter

Centre Frequency	175.42MHz
Pass Band	±1.0MHz minimum (within ±1.0dB)
Insertion loss	3dB maximum
2nd IF Image frequency at 1st IF	104.58MHz
2nd IF Image frequency at RF	1504.58MHz
Source Impedance	700Ω typical
Load Impedance	700Ω typical

The first external IF filter is connected between the output of Stage 1 and input of Stage 2. It is required to reject the image of the second IF at 104.58MHz (140 - 35.42MHz), which corresponds to an RF input frequency of 1504.58MHz. Some rejection of this frequency will have been achieved by the RF filter and the GPS antenna but it is recommended that a 1st IF filter is used to reject this image frequency further. As with the RF filter, the pass-band of this filter should be flat across the 2MHz bandwidth of the GPS Coarse-Acquisition (C/A) code signal. For most filter technologies the bandwidth will be significantly greater than this. It is important to ensure that the filter has no more than 3dB loss, otherwise the gain of the receiver will not be high enough for correct operation of the AGC in the 3rd IF stage.

The first IF filter is also used to reduce the level of interfering signals that reach the Stage 2 mixer input. Consideration should be given to any interfering signals that may be present within approximately ±200MHz of the wanted GPS signal of 1575.42MHz. As with the RF filter, the first IF filter should reject any out-of-band interference to a level, at the Stage 2 mixer input, of at least 10dB below the level at which the mixer gain compresses by 1dB (refer to GP2010 data-sheet for 1dB compression level).

The Stage 1 mixer output needs external DC bias to achieve maximum IF signal handling headroom. The first IF filter should incorporate DC connections to Vcc for this, and can normally be achieved by pull-up inductors. However, the signal path from the Stage 1 to Stage 2 *must* be AC coupled. In typical applications, a two resonator coupled-tuned LC filter can be used for the 1st IF filter. Fig. 13 shows a typical design, implemented on the GP2010 Demonstration Board. This design approximates to a 2-pole Chebyshev response with 0.1dB ripple, which has good band-stop attenuation. It also has acceptable group-delay in the GPS signal band, due to the wide bandwidth of the passband (~15MHz within ±3dB).

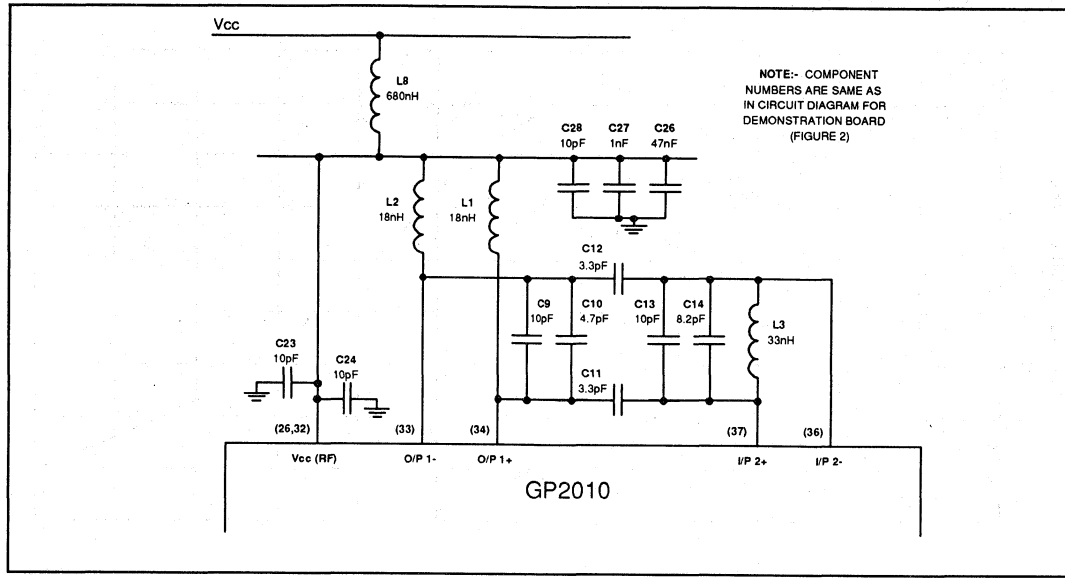


Fig.13 Typical coupled-tuned LC 1st IF filter used with GP2010, including decoupling

This IF filter is centred on 175.42MHz, with a nominal 3dB bandwidth of 15MHz. A typical frequency response for this type of filter is shown in fig.14.

The IF filter comprises the following components:-

L1,L2 - 18nH, 2%
L3 - 33nH, 2%
C9 & C10 - 14.7pF, 2% (made up of capacitors in parallel)
C13 & C14 - 18.2pF, 2% (made up of capacitors in parallel)
C11,C12 - 3.3pF, 2%

Inductors L1, 2 and 3 should have a Q of greater than 30 at 175.42MHz, and a self-resonant frequency of greater than 1500MHz.

These filter components need to have a close tolerance to ensure that the frequency response of the filter remains acceptable over the tolerance of component manufacture - 2% tolerance is preferable to 5%. It may be necessary to adjust the values of these components to ensure the filter-response is maintained from device to device

ALL other components are for decoupling purposes. Since the Stage 1 mixer has a double-balanced design, there is high rejection of local-oscillator and RF input signals at the mixer output. However, the filter needs to supply DC bias to the Stage 1 mixer output, and for this reason it is crucial to ensure that the IF filter Vcc is well decoupled over a wide frequency range. A decoupling inductor is used to achieve this (L4 = 680nH) in conjunction with wide-band decoupling capacitors (C28 = 10pF, C27 = 1nF, and C26 = 47nF).

The layout of the filter on a PCB is fairly critical, since any change in separation of the components can affect inter-component parasitics, and hence the response of the filter. It is worth ensuring that balanced signal tracks are kept close together and have the same length for each of the two signal lines. Allowance should be made to ensure there is good isolation between the filter and the RF input signal track.

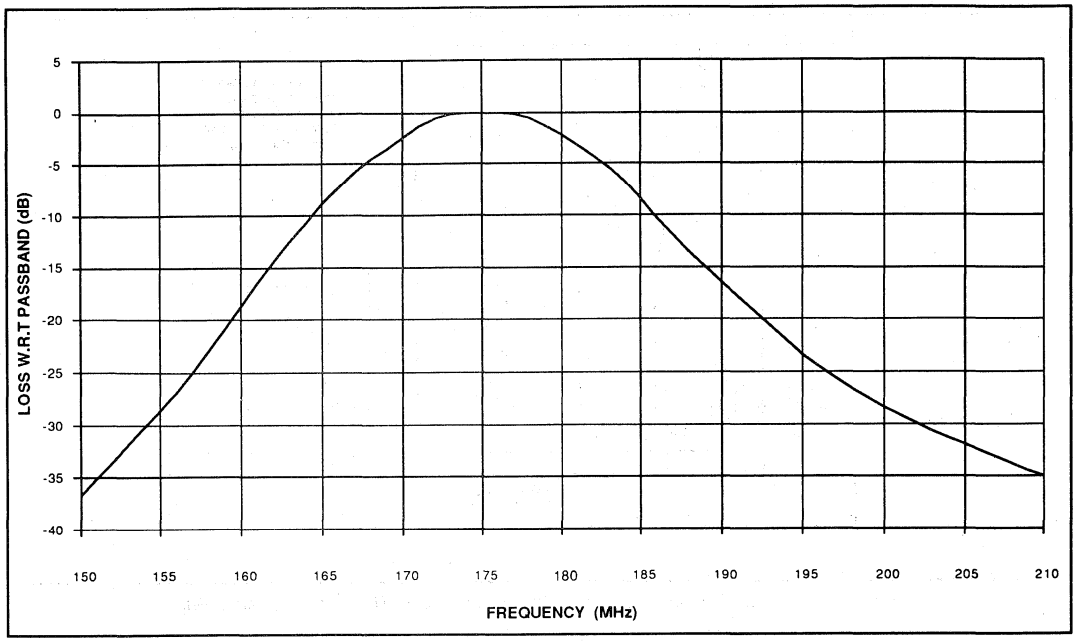


Fig.14 Typical frequency response of 1st IF filter

2nd IF filter

Centre Frequency	35.42MHz
Pass Band	±1.0MHz (within ±1.0dB)
Insertion loss	3 to 18dB
Stop Band	>10dB within ±2.0MHz
3rd IF Image frequency at 2nd IF	26.8MHz
Group-delay ripple	<300ns (34.62 to 36.22MHz)
Maximum group-delay	<1.7µs
Source Impedance	500Ω typical
Load Impedance	1000Ω typical

The second external IF filter is connected between the output of Stage 2 and input of Stage 3. It is required to define the bandwidth of the RF section of the GPS receiver. Hence it is critical to the receiver performance. The filter should be flat across the 2MHz bandwidth of the GPS Coarse Acquisition (C/A) code signal. It should also have high rejection (greater than 20dB) beyond this bandwidth, and so should have a brick-wall type response at these extremes. This can be realised with a specifically designed SAW filter, the DW9255, available from GEC Plessey Semiconductors, (refer to Data-Sheet number DS3861).This SAW filter provides a 1dB Bandwidth of typically 1.9MHz centred on 35.42MHz, with a typical pass band ripple of 0.8dB, when the SAW input and output capacitance is resonantly matched with inductors of optimum value. The out-of-band signal rejection is better than 21dB at ±2.0MHz, and better than 35dB at ±7.5MHz.

The frequency response of the DW9255 SAW filter with matching components is shown in Fig.15.

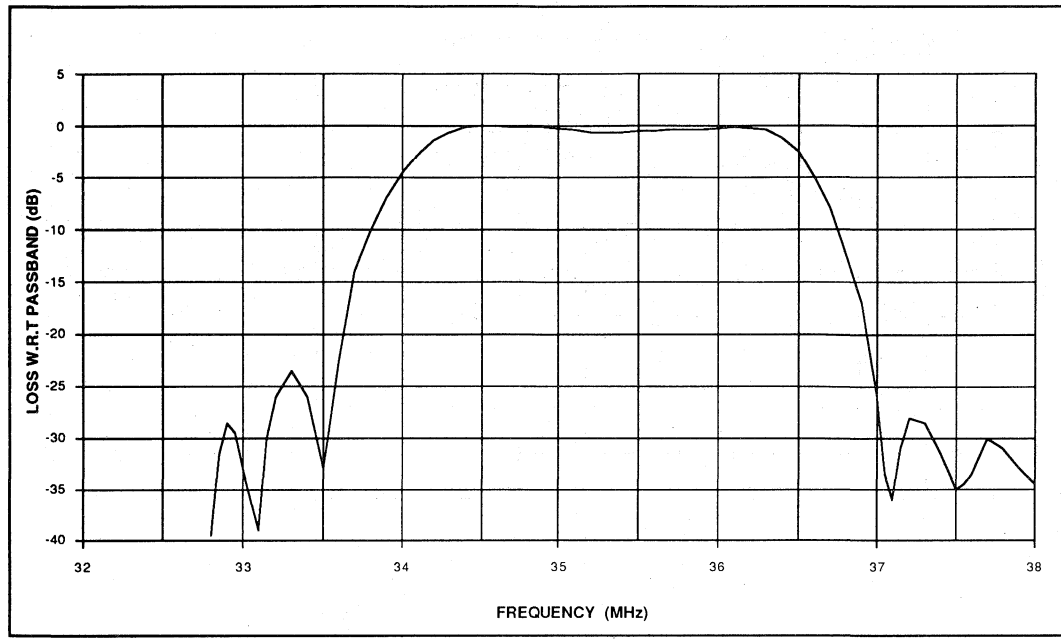


Fig.15 Typical frequency response of DW9255 SAW filter used as 2nd IF filter

3rd IF filter

Centre Frequency	4.3MHz
Pass Band	see GP2010 data sheet DS4056 - "Electrical characteristics"

The third IF filter is on-chip on the GP2010, and so cannot be user-defined. The performance of this filter is defined in the data-sheet. The overall RF bandwidth of the GPS receiver is defined by the 2nd IF filter, so the third IF filter is used to reject out-of-band noise and interference from entering the on-chip analog to digital converter. The response is essentially band pass, with a low pass operating above 10MHz, and a high-pass filter with a corner frequency of 2.0MHz which is used between the point which the IFOUT signal is connected, and the analog to digital converter. Hence, the IFOUT signal will NOT show the high-pass response.

The final IF can be monitored via the IFOUT test-point before the signal is digitised. This test-point is a high-impedance output, buffered by an on-chip 1kΩ resistor. To monitor this point, it is imperative that the signal is AC coupled, since there is a DC bias from the GP2010.

The frequency response of the third IF filter is shown in Fig.16, with 3 traces:-

IFOUT RESPONSE - spectrum observed at IFOUT pin,

ZERO RESPONSE - response calculated between IFOUT pin and analog to digital converter,

ADC I/P RESPONSE - IF spectrum of stage 3 calculated at analog to digital converter input.

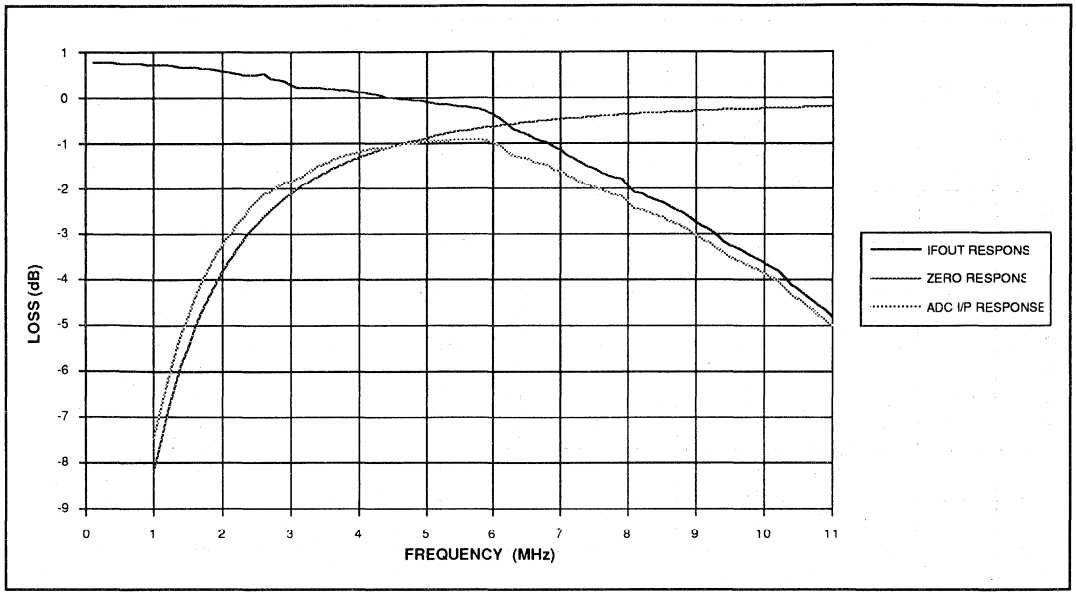


Fig.16 Typical frequency response of 3rd IF filter (on-chip)

AGC TIME CONSTANT AND MONITORING OF GAIN LEVEL

The third IF stage of the GP2010 has an Automatic Gain Control (AGC) to ensure that the level of the IF signal at the input to the Analog to Digital converter remains constant, giving a duty-cycle for the MAG data output of 30%.

In most applications, the time-constant (Δt) of the AGC can be fixed to approximately 2ms with the connection of a 100nF capacitor between pins AGC+ (pin 22) and AGC- (pin 21). However, there are now applications using "pseudolites" for aircraft landing systems where the AGC will need to have a much shorter time-constant, maybe in the order of 50µs, to cope with the huge difference in RF signal level from these and the satellites in the sky.

The time-constant of the AGC with a given capacitor ($Cagc$) connected between AGC+ and AGC- is dependent on the required gain change.

The ratio of gain adjustment ($\Delta Gain$) to the change of voltage across the AGC capacitor ($\Delta Vagc$) is approximately 400dB/V. (Although NOT linear over the whole gain adjustment range, 0.4dB/mV is a reasonable approximation).

For the case of a large interfering signal (in close proximity to a pseudolite, for example) driving the AGC to reduce gain, the recovery time after the interfering signal disappears depends upon the rate of change of $\Delta Vagc$. For large gain changes the AGC capacitor is charged/discharged by a 50µA current.

$$\frac{\Delta Vagc}{\Delta t} = \frac{50\mu A}{Cagc} \qquad \therefore \Delta t = \frac{Cagc \times \Delta Gain}{400 \times (50 \times 10^{-6})}$$

For example, a 40dB change in gain gives:-

$$\Delta Vagc = 100mV \text{ and } \Delta t = 2000 \times Cagc$$

The level of gain reduction by the AGC can be monitored by measuring the change in differential voltage across the AGC capacitor (Cagc). This voltage can also be used to drive a differential amplifier to give a voltage change with respect to 0V (Vee), see fig.17.

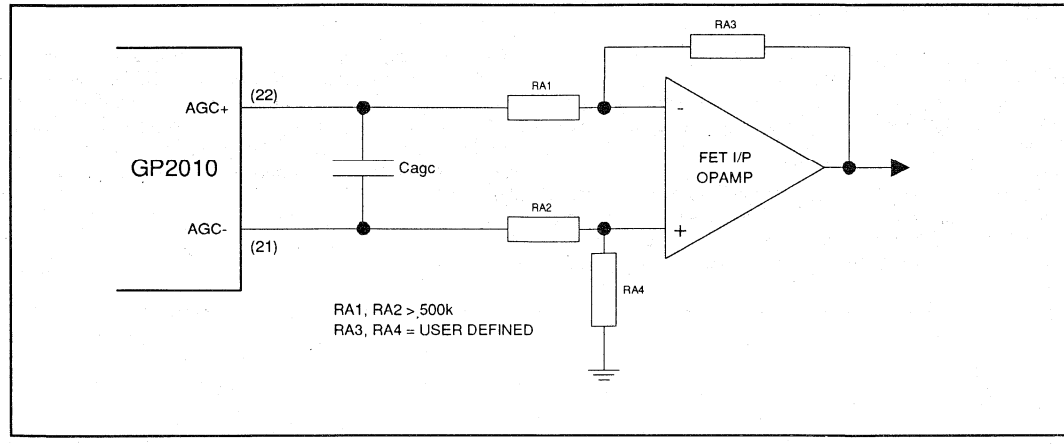


Fig.17 A differential amplifier buffer used to monitor AGC

The following points should be noted when applying this circuit to the GP2010:-

1) The output DC bias on AGC+ (pin 22) and AGC- (pin 21) can vary from Vcc to (Vcc-0.4V) maximum. The op amp should have the capability of measuring these DC voltages with a high common-mode-rejection-ratio (CMRR).

2) The load impedance of the differential amplifier must be *greater* than 1MΩ, to ensure the AGC performance is NOT affected.

3) An op amp with a very-low input offset current should be used (e.g FET input).

This circuit will *not* provide an indication of received GPS signal power, because this is buried in the background noise over a 2MHz bandwidth. A change in AGC differential voltage will provide an indication of jamming signals and whether the front-end LNA (connected between the antenna and GP2010) is operating. Fig.18 shows how the voltage on AGC+ (pin22) varies with respect to the voltage on AGC- (pin21), when a CW signal at 1575.42MHz is applied to the RF input of a GP2010 Demonstration Board.

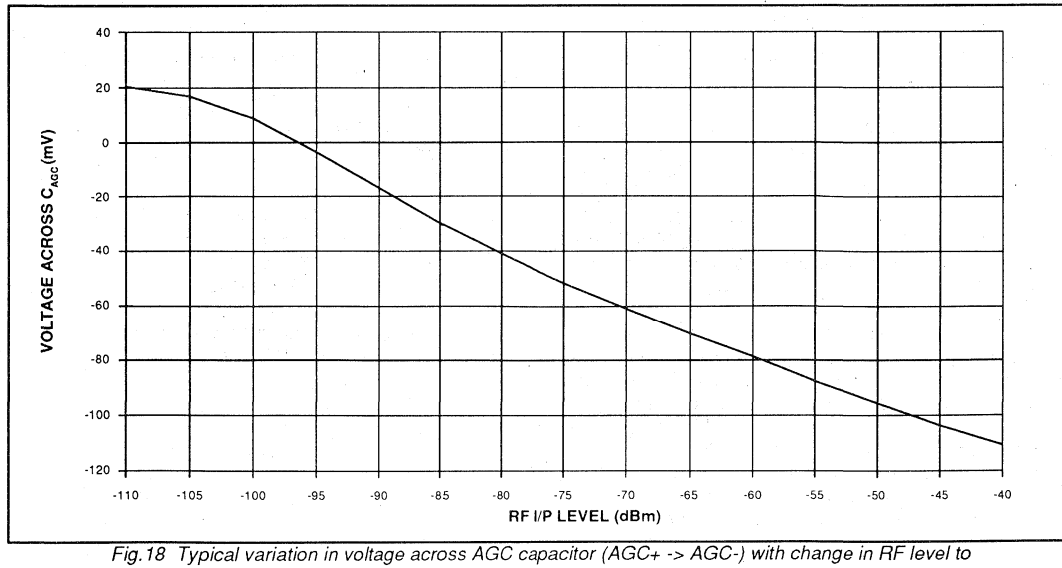


Fig.18 Typical variation in voltage across AGC capacitor (AGC+ -> AGC-) with change in RF level to GP2010 Demo board - typical at 25°C

GP2010 JAMMING SUSCEPTIBILITY

The GP2010 uses a triple-conversion frequency plan to provide a superior anti-jamming performance. The L band is increasingly being used for more RF applications besides GPS and so it will become more congested with GPS hostile signals.

The method used for showing the effects of a jamming signal applied to the RF Input of a GP2010 was to 'sweep' a jamming signal of a known power level across a pre-determined frequency spectrum combined with a GPS signal from a GPS active antenna. The GP2010 was configured as part of a complete receiver known as GPSBuilder-2, which operates with an IBM-compatible personal computer. In this configuration, the signal-to-noise ratio of a correlated GPS signal could be monitored whilst the jamming signal frequency was swept. The RF configuration used for this experiment is shown in fig.19.

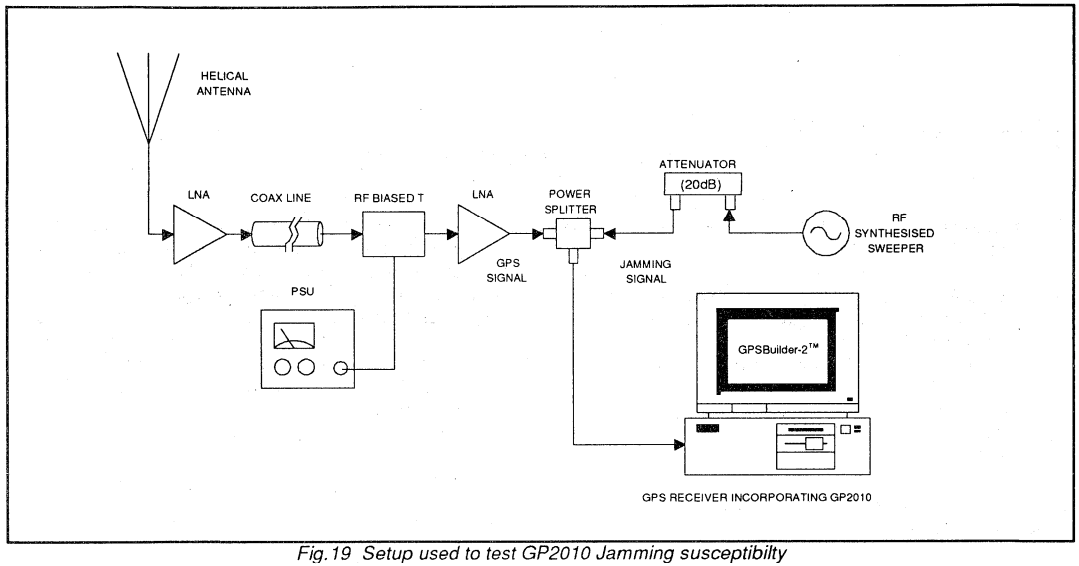


Fig.19 Setup used to test GP2010 Jamming susceptibilty

GPSBuilder-2 is available from GEC Plessey Semiconductors (refer to GPSBuilder-2 Product Brief No. DS4004).

A -40dBm signal (which simulates a very high level jamming signal) was swept from 1200MHz to 1850MHz to highlight any areas of susceptibility to jamming, with the effects being visible from the data logged signal to Noise Ratio (SNR) from GPSBuilder-2. The plot in fig. 20 shows the SNR of the GPS data from a satellite known to be in a well elevated position in the sky, and the effect of the swept jamming signal across a 1200 to 1850MHz frequency range.

Note that the GPS data SNR is very poor when the jammer is at 1224.58MHz (the image frequency of 1575.42MHz). In fact the receiver loses the GPS data completely in this instance. This is due to the AGC in Stage 3 adjusting the gain for the jamming signal, and so the noise in which the GPS data is buried will see insufficient gain in the GP2010 to give a valid data output. Also, the Stage 2 mixer will go into gain compression. The same is also true when the jammer is at 1575.42MHz which is the L1 band signal frequency.

The plot in fig.20 should be used as a guide for when the GP2010 is likely to encounter interference signals (e.g. from Mobile phones (PDC)). The jamming resistance is very good unless jamming singals appear at the following frequencies (within ±3MHz):-

1224.58MHZ
1295.42MHz
1435.42MHz
1504.58MHz
1575.42MHz

All these frequencies produce a component at the IFOUT (pin 1) at a frequency of 4.309MHz

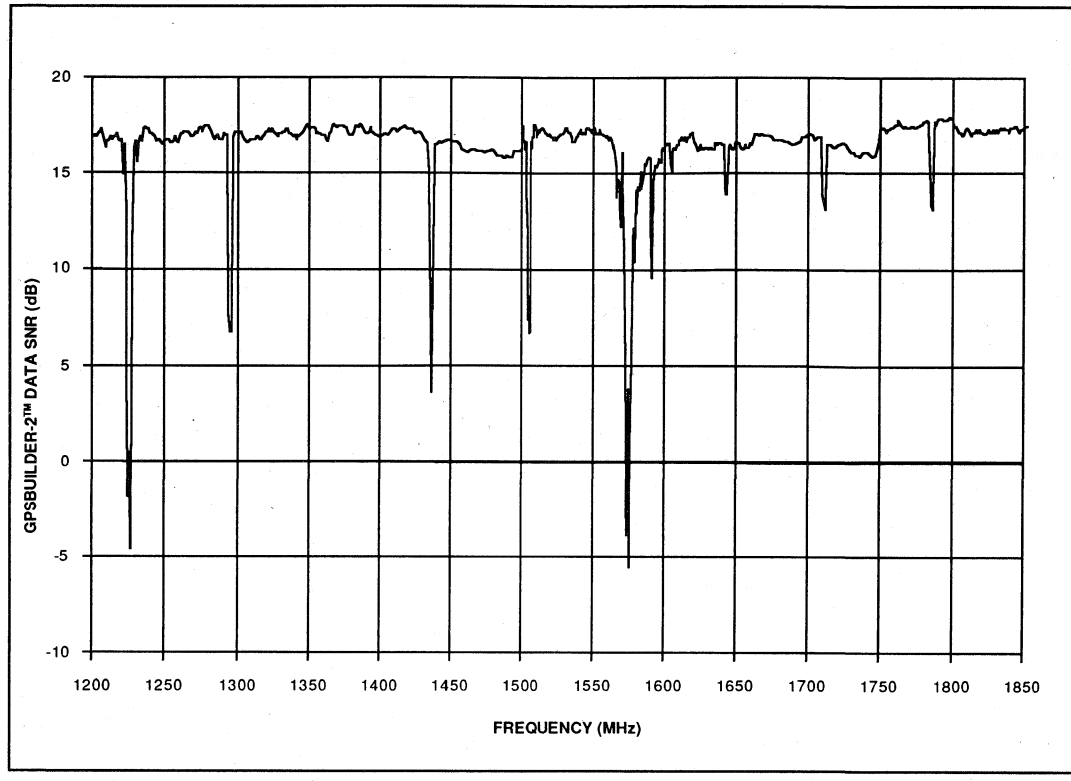


Fig.20 Correlated GPS data Signal to Noise with a swept -40dBm Jamming signal across 1200MHz to 1850MHz

An interference signal at 1224.58MHz is unlikely due to its closeness to the L2 band GPS signal frequency at 1227.6MHz.

There is a dip in the response at 1504.58MHz, because this frequency mixes down to 104.58MHz at the first IF, where it becomes the image of the second IF. 1295.42MHz similarly mixes down to 104.58MHz at the first IF. The effect of both frequencies can be reduced by increasing the rejection of the first IF filter at 104.58MHz.

In any application where high-energy, out-of-band interference signals are expected at the RF i/p (pin 29) of the GP2010, it is best to try and filter out the signals before they enter the RF I/P. This can be achieved by cascading multi-pole ceramic filters in the RF signal line. It is vital that the amplitude of any RF interference signal is kept well below the minimum specification for Mixer 1 1dB Gain Compression (10dB below gives good margin) - refer to GP2010 datasheet - Electrical Characteristics. Otherwise, the GP2010 will gain -compress on the interference signal, and hence gain-compress the wanted GPS signal.

DESIGN WITH THE GP2015

(This Application Note should be used in conjunction with the GP2015 Datasheet, DS4374)

The GP2015 is a complete RF front-end for the Global Positioning System (GPS). A complete GPS receiver can be constructed with the addition of an active antenna with low noise amplifier (LNA), a GPS correlator IC (GP2021), a microprocessor and associated memory. A block diagram of a typical application circuit for the GP2015 appears in fig. 1.

The GP2015 device converts the direct-sequence spread-spectrum signal in the L1 band (1575.42MHz) from a GPS antenna via a low-noise amplifier to a final IF at 4.309MHz, which is then digitised into a 2-bit data-stream. An on-chip phase-locked loop (PLL) is used to provide the local-oscillator frequencies to the mixers, which can be locked to a 10.000MHz reference signal from a variety of sources. A temperature compensated crystal oscillator (TCXO) is a preferred reference frequency source, allowing superior GPS signal tracking.

The GP2015 has been designed to operate with an active antenna with a gain of *greater* than +16dB (at 1575.42MHz).

A detailed description of the GP2015 Integrated Circuit is given in the GP2015 data-sheet (No. DS4374).

APPLICATION CIRCUIT

The GP2015 GPS RF Front-end can be evaluated using the GPSBuilder-2.1 GPS development system (datasheet available from GEC Plessey Semiconductors - DS 4537). The 48 pin GP2015 RF Front-end, GP2021 correlator and ancillary components are all mounted on a double-sided printed circuit board (PCB).

This application note concentrates on the function of the GP2015 on its own, with consideration given to the interaction of other components in a typical GPS receiver.

A PCB artwork has been generated for a typical RF application circuit, which can be used successfully with the GP2015 in most GPS receiver designs. The details in this application note centre on the performance of this PCB design.

The application circuit consists of:-

- The GP2015 GPS RF front-end integrated circuit
- IF Bandpass filters centred at 175.42MHz (coupled-tuned LC) and 35.42MHz (SAW)
- PLL loop filter (15kHz bandwidth)
- PLL loop - unlock indicator
- Vcc level-sensing potential ladder
- AGC filter capacitor
- RF input matching components
- Power - supply decoupling components

Note:- there is no facility provided on the layout for RF input filtering, DC feed to an active antenna, or PLL reference signal generation.

A diagram showing the connections typically needed to a GP2015 in a GPS receiver using the GP2021 correlator is shown in fig. 1. Note that the GP2015 is designed to operate with an Active Antenna only (or a passive antenna with LNA). A Passive antenna without LNA will not allow the GP2015 to operate reliably! (See section "Antenna Details" for further information).

A detailed circuit diagram of the GP2015 applications circuit appears in fig. 2, and the layout of a suitable PCB in fig. 3.

Although there is no digital circuitry associated with the GP2015 in this applications circuit, the layout can be implemented in any GPS receiver design, with no degradation in RF performance. Layout files are also available from GEC Plessey Semiconductors, if required.

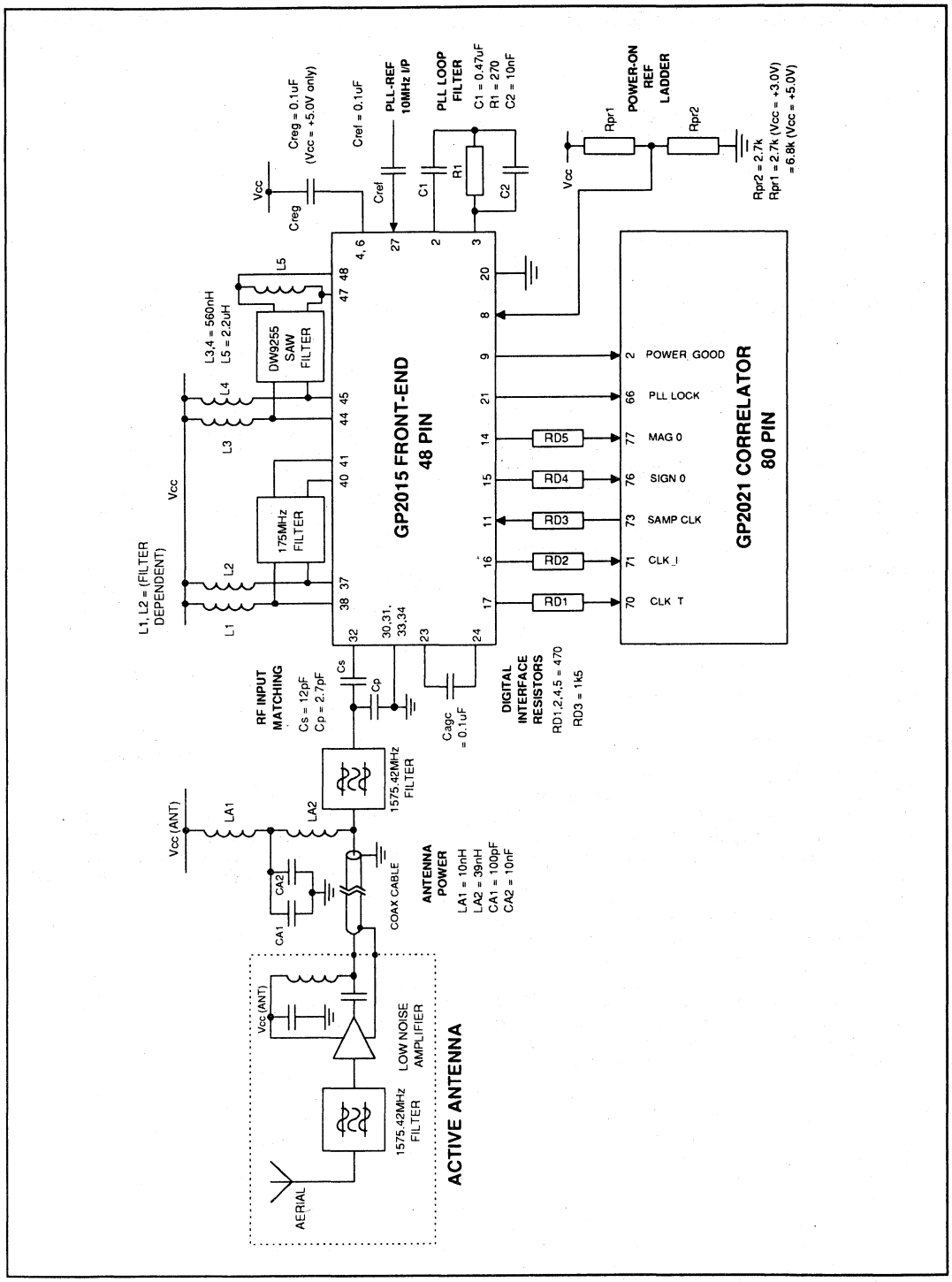
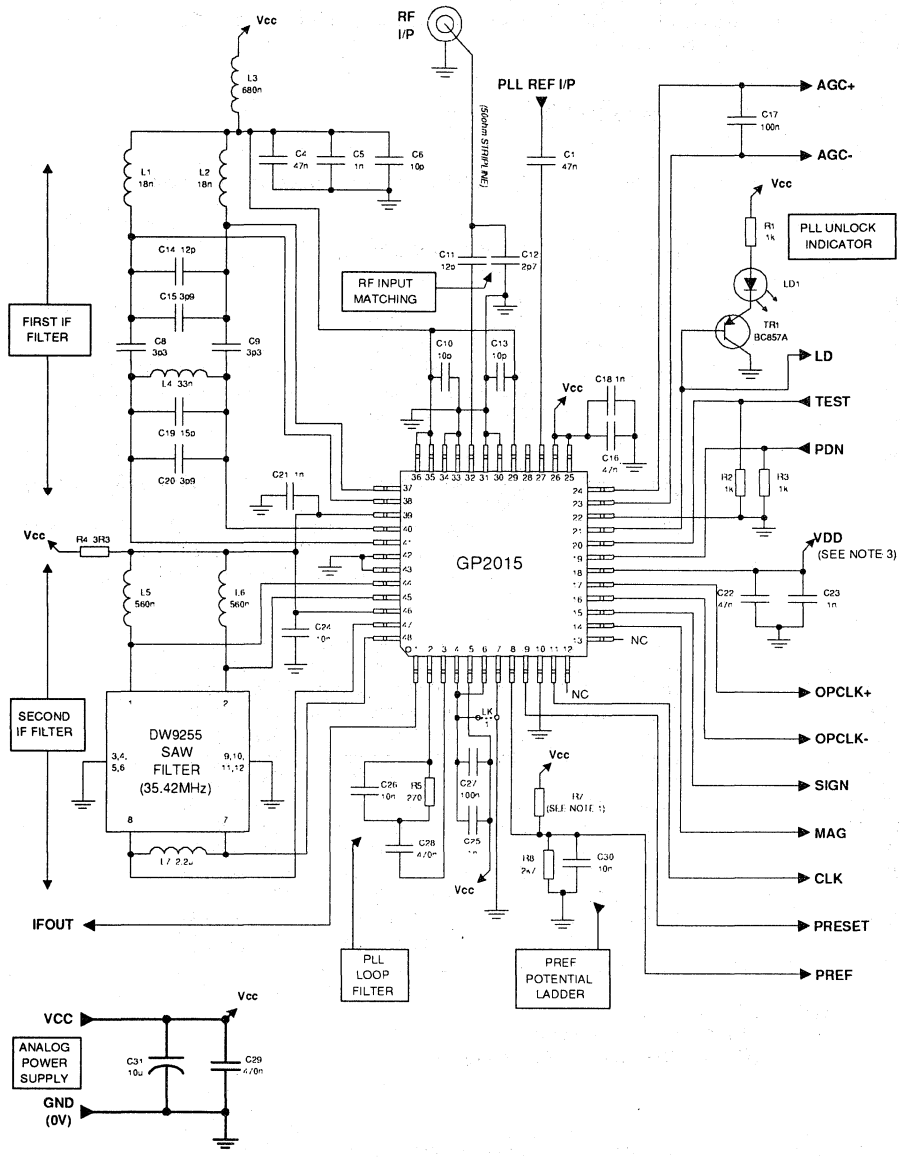


Fig.1 Typical GPS receiver RF application circuit (correlator detail NOT included)



Notes:-

1) PREF potential ladders. For Vcc = +3.0V (±10%) make resistor R7 = 2k7Ω
For Vcc = +5.0V (±10%) make resistor R7 = 6k8Ω

2) VCO Regulator can be DISABLED by making link LK1. This is MANDATORY for Vcc = +3.0V (±10%)

3) Power supply to VDD(IO) (pin 18). This supply pin should be sourced from the same PSU used for the GP2021 correlator. In this way, the VCC supply (which sources the remaining PSU pins of the GP2015) remains as clean as possible. It is possible to drive VDD (IO) from VCC supply if resources are limited, but there will be a degradation in spurious rejection in the final IF of the GP2015.

4) PLL reference (10MHz). This application circuit is configured to drive the PLL reference i/p (REF 2 - pin 27) from an external 10.000MHz reference source (e.g TCXO). It is practical to uses a crystal reference (ref fig 5b), but the performance of a GPS receiver has NOT yet been verified with this.

Fig.2 GP2015 Application Circuit diagram

GP2015 APPLICATION CIRCUIT PARTS LIST

The following list of parts are used with the GP2015 device in application, as defined in the circuit-diagram in fig. 2. Surface-mount components are used wherever possible:-

IC

		GP2015 GPS Front-end device			

SAW

		DW9255	35.42MHz SAW - 2MHz passband (s. mount)		

RESISTORS

R1		1kΩ	5%,	0.25W, 1206 chip	
R2, 3		1kΩ	5%,	0.25W, 0805 chip	
R4		3r3Ω	1%,	0.063W, 0603 chip	
R5		270Ω	1%,	0.063W, 0603 chip	
R6		51Ω	2%,	0.25W, 0805 chip	
R7	either	6k83	5%,	0.25W, 0805 chip	For Vcc = +5.0V (±10%)
	or	2k7Ω	5%,	0.25W, 0805 chip	For Vcc = +3.0V (±10%)
R8		2k7Ω	5%,	0.25W, 0805 chip	

INDUCTORS

L1, 2	18nH	5%,	0805 chip	(COILCRAFT 1008CS-180XJBC) (See Note 1)
L3	680nH	5%	1008 chip	
L4	33nH	5%,	0805 chip	(COILCRAFT 1008CS-330XJBC) (See Note 1)
L5, 6	560nH	10%,	0805 chip	(TDK MLF2012DR56KT) (See Note 2)
L7	2u2H	10%,	0805 chip	(TDK MLF2012A2R2KT) (See Note 2)

CAPACITORS

C1,4, 16, 22	47nF	10%,	25V,	0603 chip ceramic (See Note 3)
C6, 10, 13	10pF	10%,	50V,	0603 chip ceramic (See Note 3)
C5, 18, 23, 25	1nF	10%,	50V,	0603 chip ceramic (See Note 3)
C8, 9	3.3pF	±¼%,	50V,	0402 chip ceramic (See Note 3)
C11	12pF	5%,	50V,	0603 chip ceramic (See Note 3)
C12	2.7pF	±¼%,	50V,	0603 chip ceramic (See Note 3)
C14	12pF	5%,	50V,	0402 chip ceramic (See Note 3)
C15, 20	3.9pF	±¼%,	50V,	0402 chip ceramic (See Note 3)
C17, 27	0.1µF	10%,	25V,	0805 chip ceramic (See Note 3)
C19	15pF	5%,	50V,	0402 chip ceramic (See Note 3)
C21	1nF	10%,	50V,	0402 chip ceramic (See Note 3)
C24, 26	10nF	10%,	50V,	0603 chip ceramic (See Note 3)
C28, 29	0.47µF	10%,	16V,	1206 chip ceramic (See Note 3)
C30	10nF	10%,	50V,	0805 chip ceramic (See Note 3)
C31	10µF	20%,	16V,	2412 chip tantalum

OTHER COMPONENTS

LED1	AlGaAs Red LED (s. mount)
TR1	BC857A PNP transistor (s. mount)

NOTES:-

1) COILCRAFT or similar high performance inductors are recommended for the first IF filter
2) SCREENED inductors must be used for the second IF filter. Digital interference is easily picked up by L4, L5 and L6 unless they are magnetically screened.
3) ALL ceramic capacitors should use NPO, COG or X7R dielectric for high stability over temperature

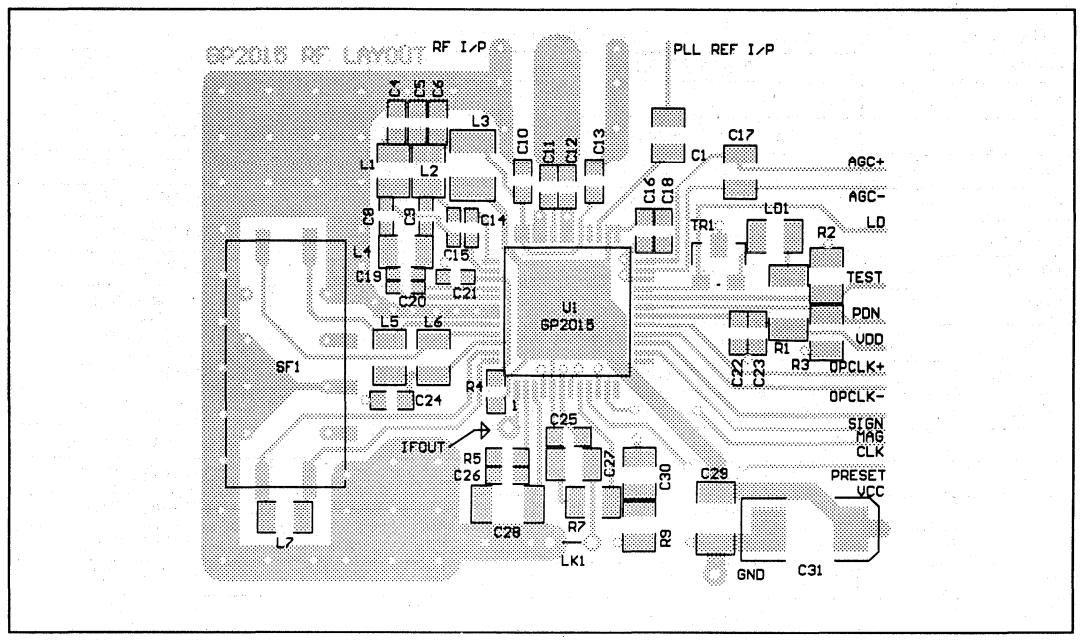


Fig.3(a) Layout of application circuit - component positions on upper layer (Not to scale)

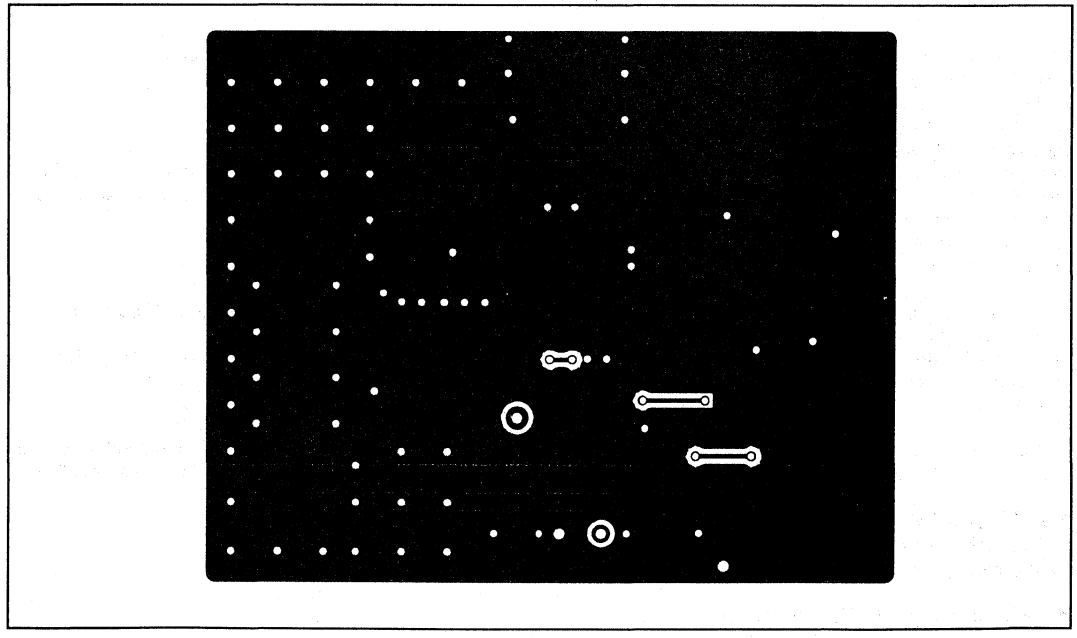


Fig.3(b) Layout of application circuit - lower copper layer (=ground plane) - Not to scale

Full details of the PCB layout are available from GEC Plessey Semiconductors. Note that the GP2015 will NOT function reliably unless a ground plane is positioned on the lower of the PCB.

OPERATING NOTES

The GP2015 Application circuit is provided with the following I/O connections:-

NAME	DESCRIPTION	I/O TYPE	CONNECT TO
GND	0v supply	INPUT	POWER SUPPLY
Vcc	+ve supply to RF section	INPUT	POWER SUPPLY
Vdd	+ve supplt to Digital interface	INPUT	POWER SUPPLY
CLK	Sample Clock input (5.71MHz)	INPUT	CORRELATOR
PRESET	Vcc level sense output	OUTPUT	CORRELATOR
IFOUT	IFOUT test point	OUTPUT	(TEST POINT)
MAG	Magnitude bit digital output	OUTPUT	CORRELATOR
SIGN	Polarity bit digital output	OUTPUT	CORRELATOR
OPCLK+	40MHz clock positive output	OUTPUT	CORRELATOR
OPCLK-	40MHz clock negative output	OUTPUT	CORRELATOR
PDN	Power-down activation input	INPUT	(USER-DEFINED)
TEST	PLL de-activation input	INPUT	(USER-DEFINED)
LD	PLL lock detect output	OUTPUT	CORRELATOR
AGC-	AGC control negative	MONITOR	(TEST POINT)
AGC+	AGC control positive	MONITOR	(TEST POINT)
RF INPUT	RF signal input at 1575.42MHz	INPUT	ACTIVE ANTENNA

The GP2015 is designed for operation from either +5.0V (±10%) or +3.0V (±10%) power-supply, although intermediate supply voltages can be used with care.

VCO SUPPLY REGULATOR

The GP2015 has an on-chip voltage regulator to provide an improved power-supply-rejection-ratio (PSRR) to the VCO. The regulator provides a +3.3V supply to the VCO when used with supply voltages (Vcc) of greater than +4.0V. It is strongly recommended that the VCO regulator is used where possible, in order to improve spurious rejection in the VCO. An improvement of 25dB in the PSRR of the VCO can be achieved using the regulator, over the 100Hz to 1MHz frequency range.

If the supply voltage (Vcc) is less than +4.0V, the function of the VCO regulator cannot be guaranteed, and so it should be disabled (refer to GP2015 data-sheet, fig.7). This is achieved by connecting VEE(OSC) (pins 4 & 6) to VEE(REG) (pin 7) or 0V.

A link (LK1) on the application circuit (see Note 2, in fig. 2) allows VEE(OSC) (pin 6) to be shorted to 0V.

5.0V OPERATION

To operate the GP2015 from +5.0V, the following connections are needed:-

- 0V DC connection to GND INPUT pin
- +5.0V DC connection to Vcc INPUT pin
- 5.71MHz digital clock connection to CLK INPUT pin (CLK low <+0.5V, CLK high >+2.0V)
- RF signal at 1575.42MHz connected to RF INPUT SMA socket.
- Power-on Reset (PREF) potential ladder - R7 set to 6k8Ω (see Note 1, in fig. 2)

3.0V OPERATION

To operate the GP2015 from +3.0V, the following connections are needed. They differ from those for +5.0V operation:-

- 0V DC connection to GND INPUT pin
- +3.0V DC connection to Vcc INPUT pin
- 5.71MHz digital clock connection to CLK INPUT pin (CLK low <0.5V, CLK high >2.0V)
- RF signal at 1575.42MHz connected to RF INPUT SMA socket.
- Power-on Reset (PREF) potential ladder - R7 set to 2k7Ω (see Note 1, in fig. 2)
- VCO voltage regulator *must* be disabled - connect VEE(OSC) (pin 4 & 6) to 0V using LK1 (see Note 2, in fig. 2)

PLL TEST INPUT

The GP2015 is provided with a TEST input, which when set to logic high (>2.0V) will *unlock* the PLL, and the VCO will operate at its highest frequency.

In normal operation, the TEST input must be at logic low (<+0.5V), which can be achieved easily by connecting TEST to 0V directly or via a 1kΩ resistor.

POWER-UP AND POWER-ON RESET CIRCUIT

On power-up, the LED which is driven from the LD output line should blink ON once, then remain OFF, as the on-chip PLL locks to the 10.000MHz reference. Also, the power-on reset (PRESET) output should toggle from logic low (0V) to logic high (Vcc). PRESET will remain at logic high unless the supply voltage reduces significantly, causing the voltage applied to the PREF input to drop below +1.21V. If the supply voltage should reduce then the PRESET output will set to logic low, indicating a power-supply failure.

A potential divider for use with the PREF input (pin 8) is shown in fig.4.

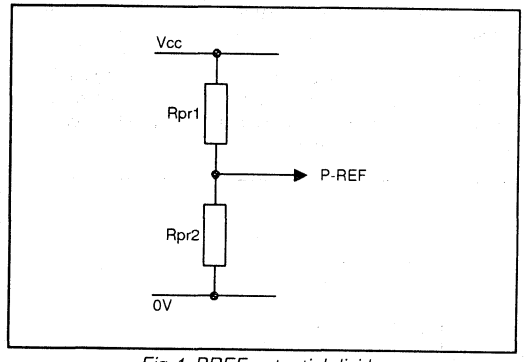


Fig.4 PREF potential divider

The value of supply voltage (Vcc(thresh)) at which the PRESET output toggles can be adjusted by changing the values of resistor in the PREF potential divider, as per the formula:-

$$Vcc(thresh) = \frac{1.21V \times (Rpr1+Rpr2)}{Rpr2}$$

The values used with the demonstration board (refer to fig.2) are:-

i) Vcc = +5.0V, Rpr1 = R7 = 6k8Ω & Rpr2 = R8 = 2k7Ω, giving Vcc(thresh) = +4.25V.

ii) Vcc = +3.0V, Rpr1 = R7 = 2k7Ω & Rpr2 = R8 = 2k7Ω, giving Vcc(thresh) = +2.42V.

The correct PLL frequency can be monitored from the OPCLK+ & OPCLK- output pins. The signal from these will be exactly 40MHz when the PLL is locked correctly (1400MHz divided by 35), at a level of approximately 100mV peak-to-peak. The two OPCLK pins give a balanced differential 40MHz output.

POWER DOWN (PDN) INPUT

The GP2015 is provided with a PDN input, which when set to logic high (>+2.0V) will power-down ALL the chip functions (except for the Power-on Reset function) resulting in a greatly reduced current consumption.

In normal operation, the PDN input must be at logic low (<+0.5V) which is easily achieved by connecting PDN to 0V directly or via a 1kΩ resistor.

ANALOG TO DIGITAL CONVERTER

By applying a digital clock to the CLK input pin, the sampled IF output will appear as a 2-bit quantised signal at the SIGN and MAG pins. The SIGN data indicates the *polarity* of the digital IF signal, and the MAG data indicates the *amplitude.* The data from the SIGN and MAG pins is in Not-Return-to-Zero (NRZ) format (hence the data is latched for the whole CLK period). The operation of the AGC in the 3rd IF stage is determined by a comparator (which operates independently of CLK) to give a MAG duty-cycle of 30% (nominal) over the AGC control range. The duty-cycle refers to the number of logic high states from MAG over a given number of CLK periods. Both MAG and SIGN data are latched on the *rising* edge of the CLK digital clock

The frequency of the sampling CLK input signal can be user-defined. When the GP2015 is used with the GP2021 correlator, the sampling frequency is 5.71MHz (40MHz divided by 7), which aliases the 4.309MHz analog IFOUT down to a 1.405MHz digital IF.

CONFIGURING A 10.000MHz PLL REFERENCE FREQUENCY

The GP2015 has an on-chip PLL, designed to multiply a 10.000MHz PLL reference signal up to 1400MHz (= on-chip VCO frequency), and divide this signal down to produce further signals:-

1400MHz	-	1st LO for mixer 1	- raw on-chip VCO output
140MHz	-	2nd LO for Mixer 2	- VCO divided by 10
40MHz	-	OPCLK for correlator	- VCO divided by 35
31.11MHz	-	3rd LO for Mixer 3	- VCO divided by 45

The GP2015 Applications circuit does NOT provide a 10.000MHZ PLL reference signal source. The GP2015 alone (without correlator connected) will operate successfully from a crystal (in conjunction with an on-chip crystal-oscillator) with a frequency tolerance of at least ±0.1MHz. However, the correlator requires the GP2015 to deliver a very stable frequency source to it, to allow satellite tracking to occur reliably. In most GPS receiver applications using the GP2015 (or GP2010) GPS RF Front-end and GP2021 correlator, it is recommended that a Temperature-Compensated-Crystal-Oscillator (TCXO) is used to provide the 10.000MHz PLL reference signal.

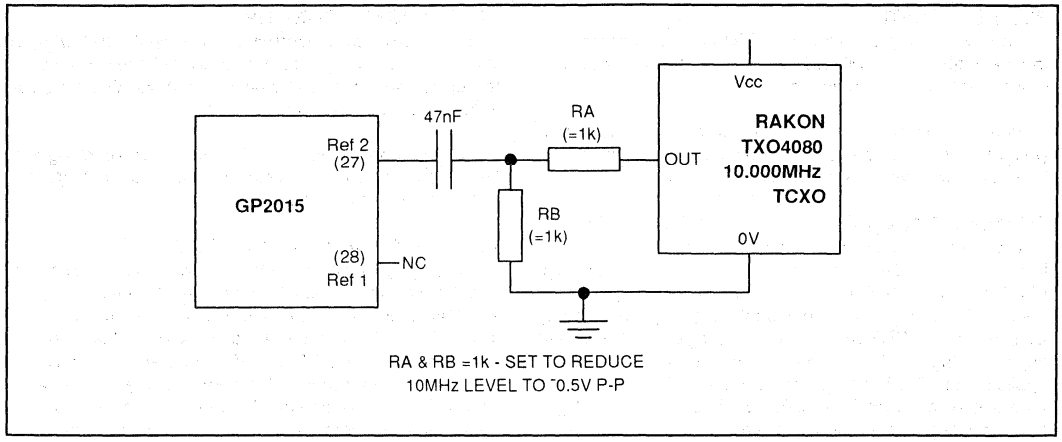


Fig.5a Rakon TCXO reference connections with 6dB attenuation

A suitable 10.000MHz TCXO is the *Rakon TXO4080*, with a 1.0V peak-to-peak *minimum* clipped sinewave output amplitude. This TCXO can be connected to the GP2015 as shown in fig. 5a, with the addition of a 6dB attenuation of this signal to produce a 0.5V peak-to-peak amplitude - optimum for the GP2015. The amplitude of the 10.000MHz frequency source *must* be > 0.1V and <1.2V peak-to-peak. If the amplitude is greater than 1.2V peak-to-peak, a spurious output may appear on the IFOUT signal (refer to section "Spurious signals in the IF spectrum"). In this case the signal should be attenuated.

Note that REF1 (pin 28) must not be connected in this instance, since this pin is a part of the on-chip crystal-reference oscillator, which is not utilised when using an externally generated source.

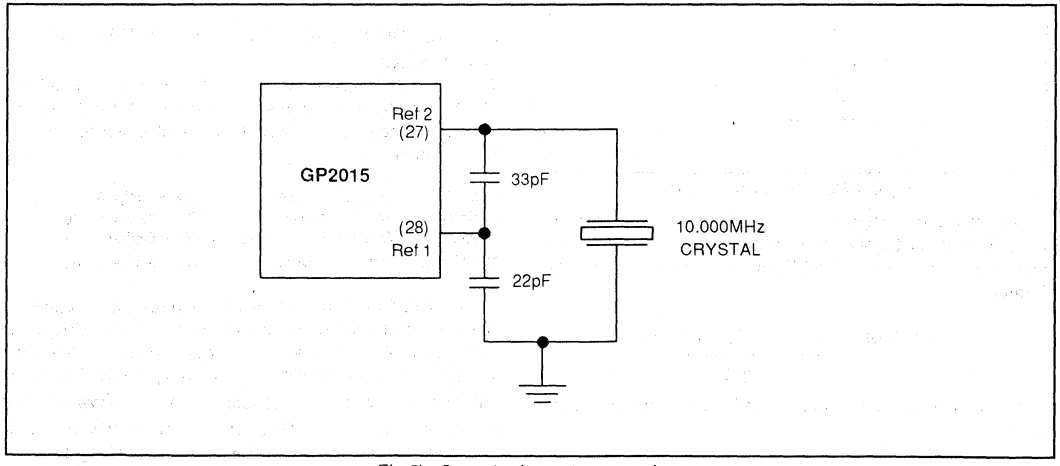


Fig.5b Crystal reference connections

The 10.000MHz PLL reference frequency can be provided by a 10.000MHz crystal in conjunction with the on-chip crystal oscillator. The crystal can be connected to the GP2015 as shown in fig. 5b. The crystal is parallel-resonant with the oscillator, and hence requires tuning capacitors in parallel as shown. The poor stability of crystal compared to a TCXO may be a problem in some applications.

PLL LOOP FILTER AND VCO PERFORMANCE

The GP2015 has an on-chip PLL to produce all the local-oscillator frequencies for the IF mixers. The recommended PLL loop filter produces a third-order PLL with a second-order external filter comprising 2 capacitors and 1 resistor, as shown in fig.6.

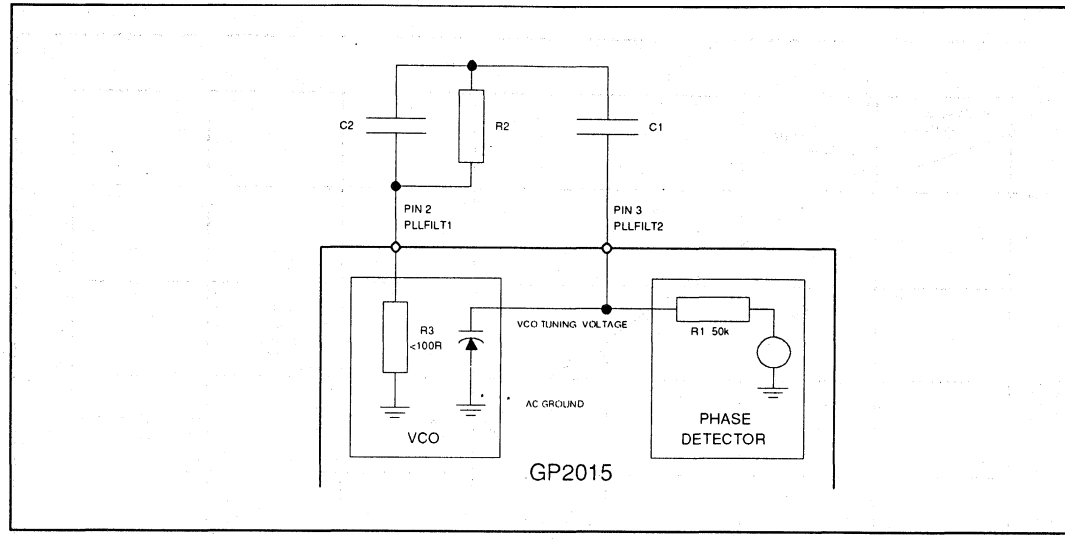


Fig.6 PLL loop filter showing relevant on-chip components

The loop filter is used to roll off the response of the PLL at high frequency, but maintain loop stability at the loop-bandwidth frequency (where loop gain = 1 (0dB)). The optimum values for this PLL loop filter can be calculated knowing the loop-gain, phase-margin and required loop bandwidth.

The loop gain at 1radian/second can be calculated as a ratio (NOT dBs) as follows:-

$$\text{Loop Gain } (G_L) = \frac{K_D K_V}{N}$$

where :- K_D = Phase detector gain
K_V = VCO gain
N = Loop division ratio (140)

G_L is between 3.1×10^6 and 100×10^6 for the GP2015 (130dB and 160dB).

Knowing the loop gain, the time-constants of the filter can be calculated as follows:-

$$\tau 1 = \frac{G_L}{\omega_n^2}\sqrt{\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}} \quad \text{.....(1)}$$

$$\tau 2 = \frac{1}{\omega_n^2\tau_3^2} \quad \text{.....(2)}$$

$$\tau 3 = \frac{-\tan\phi + \frac{1}{\cos\phi}}{\omega_n} \quad \text{.....(3)}$$

where:- G_L = PLL loop gain at 1radian/second offset
$\tau 1$ = time constant of first filter pole
$\tau 2$ = time constant of filter zero
$\tau 3$ = time constant of second filter pole
ω_n = PLL loop bandwidth
ϕ = PLL phase margin

For the PLL loop filter referred in fig.6:-

$\tau 1$ = R1C1
$\tau 2$ = R2(C1+C2)
$\tau 3$ = R2C2

Resistor R3 (on-chip) can be regarded as an AC ground since its value is much smaller than R1 (50kΩ).

The recommended PLL loop filter has the following values for external components, giving a nominal loop-bandwidth of 15kHz and phase-margin of 60°:-

C1 = 470nF
R2 = 270Ω
C2 = 10nF

The higher the phase margin (ϕ) of the loop filter at the loop bandwidth (ω_n), the higher the stability of the PLL across the full range of loop gain. The graph in fig.7 shows the loop filter response for the loop-filter components defined above, and fig.8 shows the spectrum of the 1400MHz VCO signal from a GP2015 at +25°C, with the VCO regulator enabled.

There are further components on chip which produce bandwidth limiting within the phase-detector. These provide two further poles in the PLL filter response at 400kHz (2.51Mrads/sec) and 530kHz (3.33Mrads/sec). These have negligible effect on PLL loop stability provided the PLL loop bandwidth is less than 100kHz.

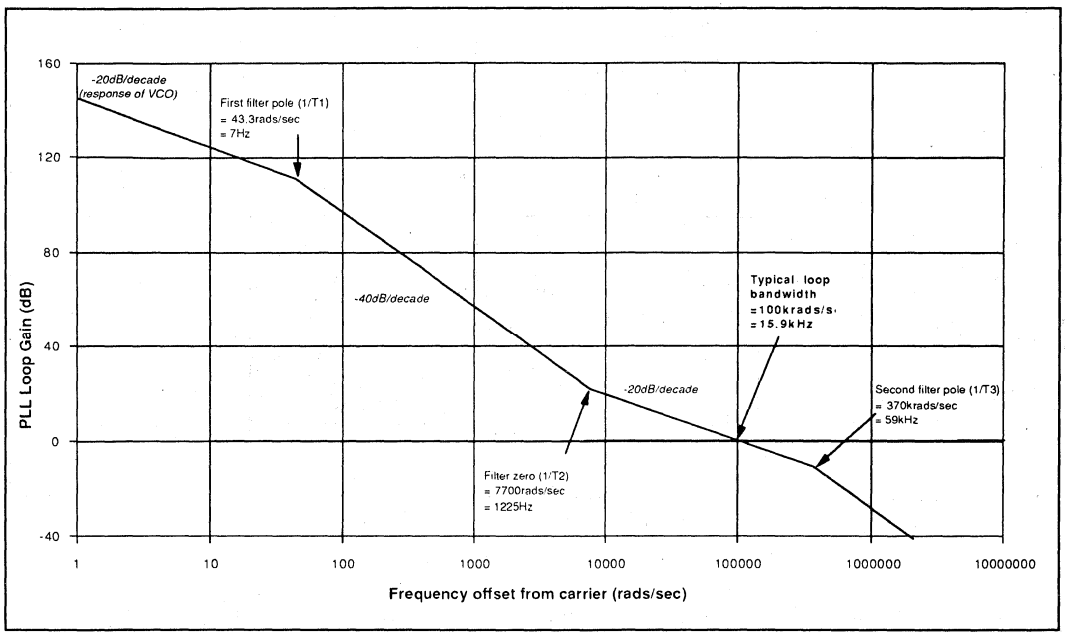


Fig.7 Typical GP2015 PLL loop gain (G_L) vs. frequency

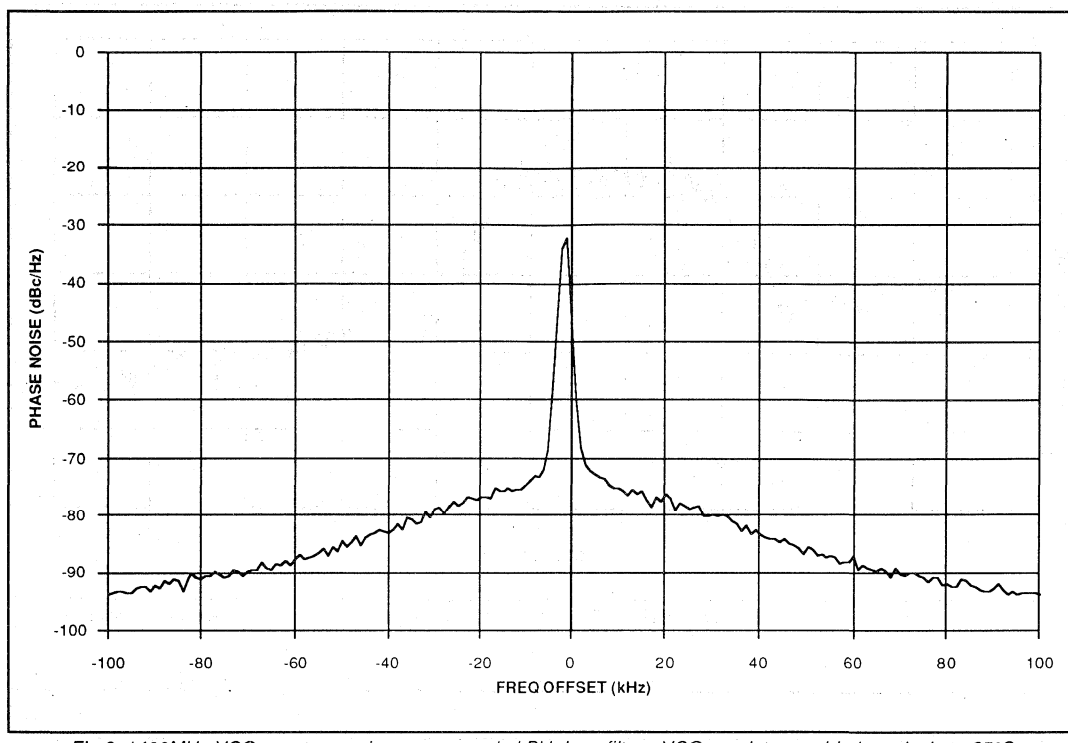


Fig.8 1400MHz VCO spectrum using recommended PLL loop filter - VCO regulator enabled - typical at +25°C

IFOUT SPECTRUM

The IFOUT output is a high impedance (1kΩ) monitor point, for test purposes only, which can be used to monitor the output of the IF chain before the analog-to-digital converter. Figs 9, 10 & 11 show typical IFOUT spectra for the GP2015, under differing operating conditions:-

Fig.9:- NO RF INPUT signal, NO 5.71MHz digital clock applied to CLK;

Fig.10:- NO RF INPUT signal applied, a 5.71MHz TTL clock applied to CLK via 1kΩ series resistor;

Fig.11:- RF INPUT signal applied from a GPS antenna with 26dB Gain and 2.5dB noise figure and a 5.71MHz TTL clock applied to CLK via 1kΩ series resistor;

Observe that the on-chip AGC suppresses the level of out-of-band noise and spurious signals as the level of noise at 1575.42MHz at the RF input increases (the GPS signal is buried in noise). The spectrum in fig.11 is typical of that produced by a working GPS receiver using the GP2015.

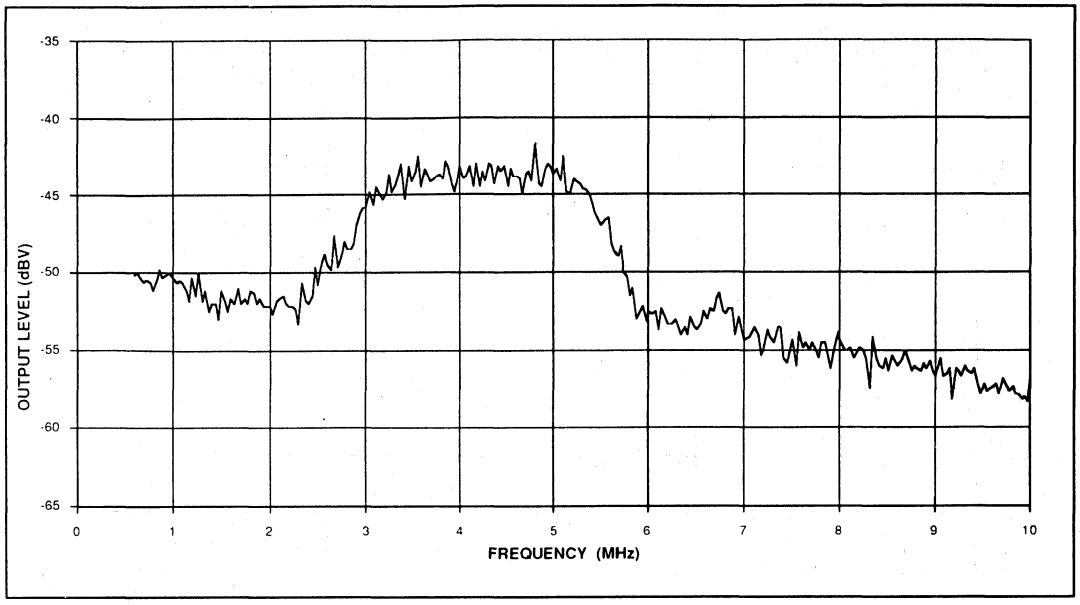


Fig.9 Typical IFOUT spectrum (Resolution BW = 300kHz) - sampling CLK disabled & no GPS antenna connected

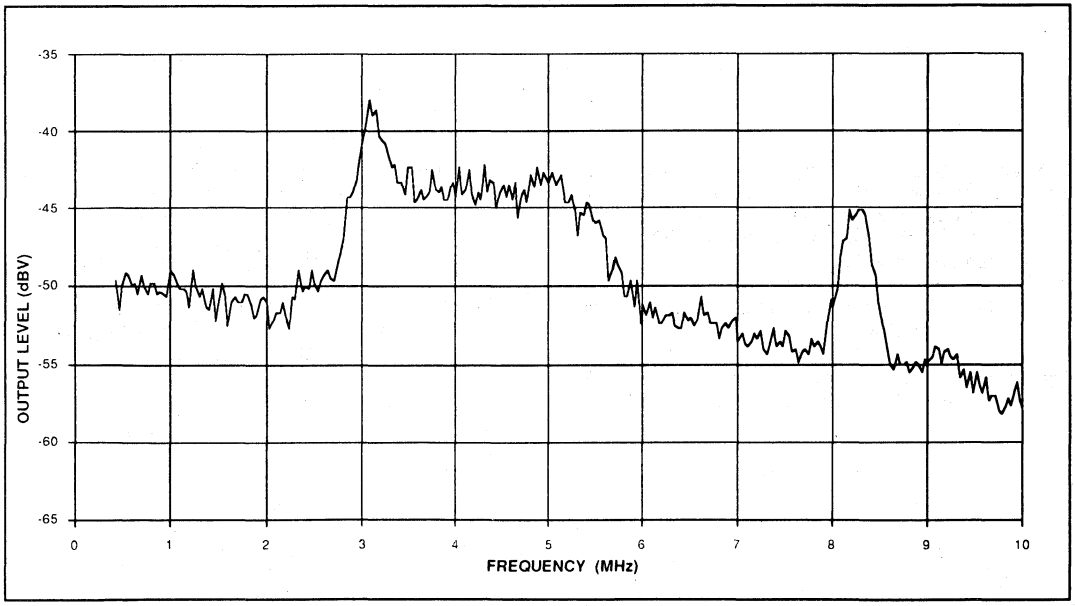


Fig.10 Typical IFOUT spectrum (Resolution BW = 300kHz) - 5.71MHz sampling CLK enabled & no GPS antenna connected

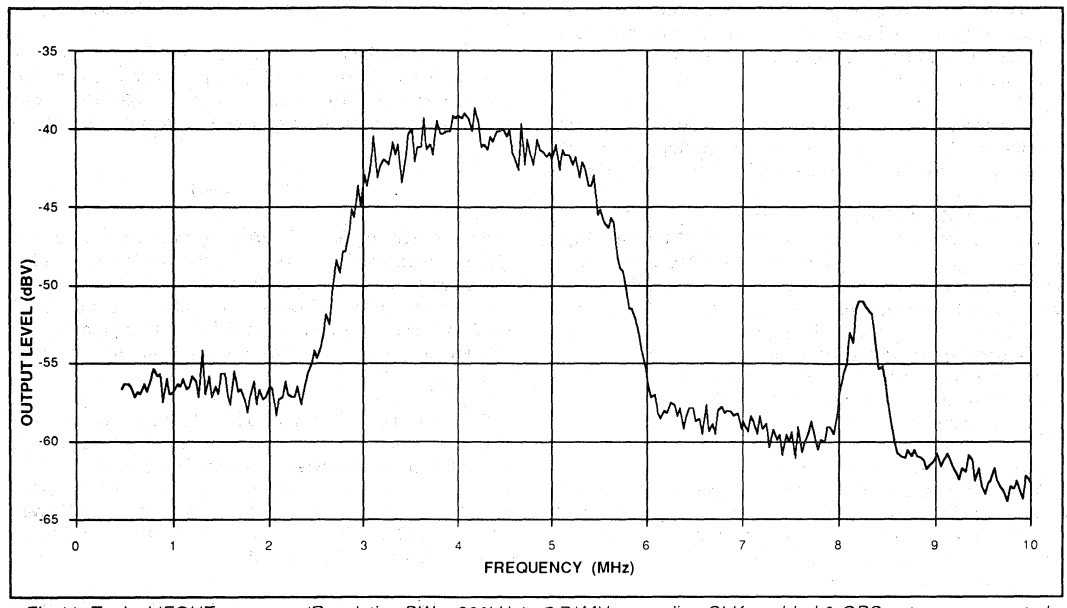


Fig.11 Typical IFOUT spectrum (Resolution BW = 300kHz) - 5.71MHz sampling CLK enabled & GPS antenna connected

SPURIOUS SIGNALS IN THE IF SPECTRUM

For the GP2015 to work correctly, the stage 3 AGC circuit should set the level of noise in the mixed-down GPS L1 band (4.309MHz ±1.023MHz) to approx 100mV r.m.s (nominal) at the IFOUT (pin 1). Any IF spurs should be suppressed to a level of *less* than -20dBc of the nominal IFOUT level to avoid the AGC attenuating the noise in the band of the mixed-down GPS L1 signal to a level which the correlator will cease to track GPS satellite signals.

The GP2015 uses a balanced-signal architecture, and is largely immune to spurious signals. However, there are some exceptions (refer to spectral plots of IFOUT in figs 10 & 11):-

Digital interference spurs, including CLK sampling the analog to digital converter.

Some digital signals can couple across the GP2015 chip independently of any peripheral components. Care should be taken to ensure that harmonics of the CLK input signal are kept to a minimum so that they do not become mixed in-band in the IF chain.

If CLK is at a frequency of 5.71MHz (typical application with GP2021), spurious signals *can* appear on the IFOUT pin at frequencies of 8.25MHz, 2.54MHz and 3.17MHz. These are due to the 4th, 5th and 6th harmonics of CLK respectively, and they can jam the AGC if they are large, and hence affect the GPS data from the MAG and SIGN outputs.

Harmonics due to CLK can be reduced by attenuating the CLK signal input to the GP2015 to a 2V amplitude using a potential divider (typical resistor values in the region of 1kΩ - dependent upon level of Vcc). An alternative method is to insert a 1k5Ω resistor in *series* with the CLK input, the upper harmonics can be rolled off by creating a pole with the input capacitance. Care should be taken to ensure that the MAG and SIGN output latches on the GP2015 do not "double-clock" (i.e. trigger on both the rising *and* falling edges of the CLK signal).

Jamming interference can also occur from the close proximity of the GP2015 to associated microprocessor and memory circuitry in a GPS receiver. This is primarily due to the sensitivity of the 3rd stage mixer with a high-value inductor used to produce the bandpass response in the 2nd IF filter. The inductor (L6) used to resonate with the DW9255 SAW filter is a high value (2.2µH) which has a high impedance at 35.42MHz (~490Ω), which has a side-effect of allowing it to operate as an effective antenna to interference at similar frequencies. L6 is particulary vulnerable to pickup as it is situated after the SAW filter, and signals injected at that point are not rejected by the SAW. The amplitude of digital jamming spurs can be reduced by using the following techniques:-

a) L4, L5 and L6 inductors around SAW filter can be magnetically - screened, monolithic multi-layer types.
b) Mount the L6 inductor inside a screening can, but take care to ensure that the self-resonant frequency and inductor Q are *not* greatly reduced.
c) Mount the L6 inductor coil in an *orthogonal* plane (vertical) to the digital tracks on the PCB.

d) Ensure that *no* power-supply and digital tracks run in close-proximity to the L6 inductor. Ideally the L6 inductor should be surrounded by ground-plane on *all* board layers for a radius of >15mm.

In practice, in all but the most extreme environments, most benefits are obtained by using screened inductors, especially for L6, and by routing power and digital tracks clear of L6.

External 10.000MHZ PLL reference

Care should be used to ensure that the 10.000MHz PLL reference signal is AC coupled into the GP2015, and that the amplitude does not exceed 1.2V peak-to-peak. If the amplitude is higher than this, harmonics of the PLL reference can interfere with the 3rd stage mixer and produce interference spurs on the signal at IFOUT (in particular the third harmonic (30MHz) will produce a spur at 1.111MHz). A suitable attenuator should be used if a TCXO with TTL level outputs is used (refer to fig.5).

Self generated spurious signals

A spurious signal at 15.55MHz exists at the IFOUT resulting from an on-chip interaction between the second and third IF stages. The spur has variable amplitude but is always sufficiently low to have no effect on the 3rd IF stage AGC, or GPS signal reception.

ANTENNA DETAILS

The GP2015 has been designed to use the signal from a GPS antenna with a low-noise-amplifier (LNA). The noise figure of the complete receiver will then be dominated by the noise figure of the LNA. However, care should be taken to ensure that the gain of the LNA is high enough to allow the GP2015 to function correctly in a GPS receiver.

The GPS signal is spread-spectrum modulated with a 2.046 MHz bandwidth, and received power is in the region of -130dBm. The power of background noise in the same bandwidth is -111dBm, so the GPS signal is buried within the background noise. The GP2015 AGC operates on the noise in the band of the GPS signal and not on the GPS signal itself. The de-spreading of the GPS signal restores a positive signal-to-noise ratio. This is carried out by a DSP correlator chip - the GP2021 is recommended.

The power of the noise over a 2MHz bandwidth is 63dB up on the noise in a 1Hz bandwidth (-174dBm/Hz), giving a minimum signal power of approximately -111dBm. Consider also the following values (with reference to the "IF filter details" section and the Electrical Characteristics table in the GP2015 Data-sheet):-

Max IF gain of GP2015 (minimum guaranteed) =106dB ...(a)
Max attenuation of external IF filters = 21dB ...(b)
Nom IFOUT level with AGC operating (Stage 3) =100mV rms ...(c)

Notes:-

a) The maximum IF gain taking account of the loading effects of the IF filtering (but excluding filter losses)

b) The attenuation is the sum of the losses in 1st and 2nd IF filters

c) 100mV rms is equivalent to -7dBm in a 50Ω load

When the background noise within a 2MHz bandwidth is applied *directly* to the GP2015 RF input (with no LNA or RF Input filter) and all IF filters included (with DW9255 SAW - Loss typ. -17dB), the minimum signal produced at the IFOUT will be:-

$$-111+106-21 = \mathbf{-26dBm}$$

For the AGC of 3rd IF stage to operate correctly on the applied signal, the signal level at IFOUT should be at -7dBm. This gives a shortfall in signal level of 19dB.

If a Low Loss 2nd IF filter is used in place of the DW9255 SAW, the minimum signal at the IFOUT will be greater than -26dBm, but will never be great enough to exclude the need for a LNA.

So an RF LNA with combined RF filter needs to provide at least 19dB more noise than would be provided by a passive antenna alone. The GPS receiver noise figure ideally needs to be kept low. Since the noise figure of the LNA will dominate the noise performance of the receiver, it is wise to use a LNA with N.F. of <3.0dB, which results in a *minimum* required LNA gain (plus RF filter loss) of **>+16.0dB.**

To a first approximation, the noise figure of the whole RF front-end in a GPS receiver will be:-

$$NF = F1 + \frac{(F2 - 1)}{G1 - L1}$$

where F1 = noise figure of Active Antenna LNA
F2 = noise figure of GP2015
G1 = RF gain of Active Antenna LNA
L1 = loss due to RF filtering and cabling after LNA

The typical noise figure of the GP2015 is quoted as 9dB. A typical noise-figure for an LNA is 2.5dB. A typical gain for the Active Antenna LNA is 26dB. The typical loss in a length of coax and associated RF filtering is variable - we shall assume 2dB for this example, with 2m coax cable.

Typical noise figure will be:-

$$2.5 + \frac{(9 - 1)}{(26-2)} = 2.83dB$$

This shows that the receiver Noise figure is dominated by the LNA in this case.

It is recommended that the LNA gain be kept to below 60dB, so as NOT to overload the GP2015.

Active GPS antennas can be of either patch or helical type. A recommended active GPS patch antenna is available from *M/A COM*- type *ANP-C-114*, which has an LNA gain of +26dB and a noise figure of ~2.5dB. If an RF filter (loss ~ -2.0dB) is connected between the antenna output and the RF Input to the GP2015, the resultant noise contribution of the LNA and filter will be in the region of **+26.5dB** - optimum for the GP2015.

(Note that the M/A-COM antenna above includes an 1575MHz ceramic resonator RF filter preceding that LNA.

IF FILTER DETAILS

The GP2015 has a triple conversion architecture. All three stages can be treated as separate blocks. User-defined filter networks can be used for IF filtering between stage 1 & 2, and between stage 2 & 3.

RF filter

The Stage 1 mixer has an on-chip image-rejection filter, with optimum pass band set at 1575.42MHz, and a rejection of the image frequency (1400-175.42MHz =1224.58MHz) of approximately 7dB. Image rejection is not critical at 1224.58MHz because this frequency is at approximately the GPS L2 frequency (1227.6MHz). So there is only noise at this frequency.

The Image filter is fixed, but can be enhanced by the addition of an external RF filter between the LNA and GP2015.

Centre Frequency	1575.42MHz
Pass Band	±1.0MHz minimum (within ±1.0dB)
RF Image frequency	1224.58MHz
Input Impedance	50Ω typical
Output Impedance	50Ω typical
Insertion loss	0.5dB -> 2.0dB

The RF filter is required to remove the 1224.58MHz image noise and to prevent overload of the Stage 1 mixer by strong out-of-band interference signals. The required performance of this filter will be influenced by any locally generated interfering signals that may be present (for example, mobile telephone). Ideally, the filter should reject any out-of-band interference to a level, at the GP2015 RF input, of at least 10dB below the level at which the Stage 1 mixer will gain compress by 1dB (refer to GP2015 data-sheet for 1dB compression level). The pass-band of this filter should be flat across the 2MHz bandwidth of the GPS C/A code signal. For most filter technologies the bandwidth will be significantly greater than this.

When specifying the RF filter, it is important to consider the filtering effect of the GPS antenna and low-noise amplifier. The majority of GPS antennas are patch types, which have a narrow bandwidth and will therefore provide some filtering. This can reduce the requirements of the RF filter used, and hence the cost of the overall receiver.

The insertion loss of the RF filter can affect the noise figure of the GP2015. The low-noise pre-amplifier which boosts the signal from the antenna to the GP2015 should be designed so that there is sufficient gain for the RF filter loss to have a negligible effect on overall noise figure.

A typical RF filter will be a dielectric type. Suitable filters are available from a range of manufacturers. A recommended type of RF filter is the *Murata DFC2 1R57 P002 BHD* which is centred on 1575.42MHz and has a 2MHz passband (-3.0dB).

The GP2015 requires components to match the input impedance to that of the RF filter output. Most filters have a 50Ω output impedance. Fig.12 shows the recommended matching circuit.

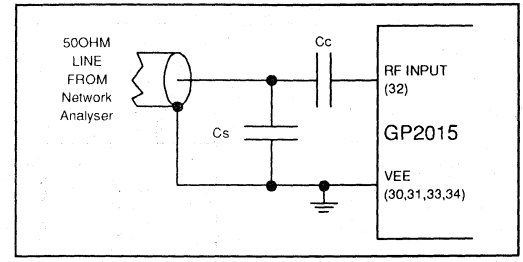


Fig.12 RF Input matching circuit

1st IF filter

Centre Frequency	175.42MHz
Pass Band	±1.0MHz minimum (within ±1.0dB)
Insertion loss	3dB maximum
2nd IF Image frequency at 1st IF	104.58MHz
2nd IF Image frequency at RF	1504.58MHz
Source Impedance	700Ω typical
Load Impedance	700Ω typical

The first external IF filter is connected between the output of Stage 1 and input of Stage 2. It is required to reject the image of the second IF at 104.58MHz (140 - 35.42MHz), which corresponds to an RF input frequency of 1504.58MHz. Some rejection of this frequency will have been achieved by the RF filter and the GPS antenna but it is recommended that a 1st IF filter is used to reject this image frequency further. As with the RF filter, the pass-band of this filter should be flat across the 2MHz bandwidth of the GPS Coarse-Acquisition (C/A) code signal. For most filter technologies the bandwidth will be significantly greater than this. It is important to ensure that the filter has no more than 3dB loss, otherwise the gain of the receiver will not be high enough for correct operation of the AGC in the 3rd IF stage.

The first IF filter is also used to reduce the level of interfering signals that reach the Stage 2 mixer input. Consideration should be given to any interfering signals that may be present within approximately ±200MHz of the wanted GPS signal of 1575.42MHz. As with the RF filter, the first IF filter should reject any out-of-band interference to a level, at the Stage 2 mixer input, of at least 10dB below the level at which the mixer gain compresses by 1dB (refer to GP2015 data-sheet for 1dB compression level).

The Stage 1 mixer output needs external DC bias to achieve maximum IF signal handling headroom. The first IF filter should incorporate DC connections to Vcc for this, and can normally be achieved by pull-up inductors. However, the signal path from the Stage 1 to Stage 2 *must* be AC coupled. In typical applications, a two resonator coupled-tuned LC filter can be used for the 1st IF filter. Fig. 13 shows a typical design, implemented on the GP2015 Demonstration Board. This design approximates to a 2-pole Chebyshev response with 0.1dB ripple, which has good band-stop attenuation. It also has acceptable group-delay in the GPS signal band, due to the wide bandwidth of the passband (~15MHz within ±3dB).

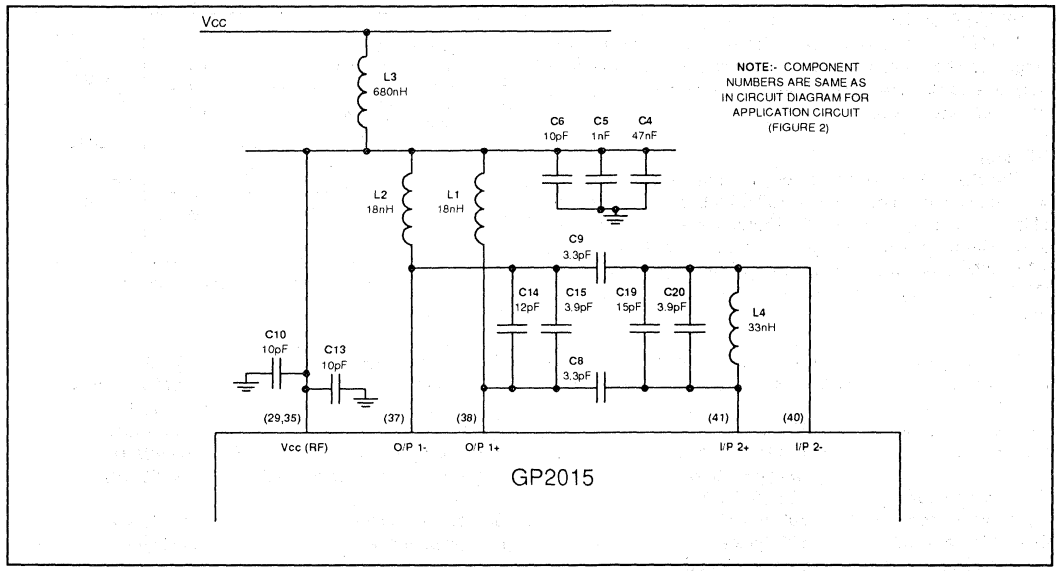


Fig.13 Typical coupled-tuned LC 1st IF filter used with GP2015, including decoupling

This IF filter is centred on 175.42MHz, with a nominal 3dB bandwidth of 15MHz. A typical frequency response for this type of filter is shown in fig.14.

The IF filter comprises the following components:-

L1,L2 - 18nH, 2%
L4 - 33nH, 2%
C14 & C15 - 15.9pF, 2% (made up of capacitors in parallel)
C19 & C20 - 18.9pF, 2% (made up of capacitors in parallel)
C8 & C9 -3.3pF, 2%

Inductors L1, 2 and 4 should have a Q of greater than 30 at 175.42MHz, and a self-resonant frequency of greater than 1500MHz.

These filter components need to have a close tolerance to ensure that the frequency response of the filter remains acceptable over the tolerance of component manufacture - 2% tolerance is preferable to 5%. It may be necessary to adjust the values of these components to ensure the filter-response is maintained from device to device

ALL other components are for decoupling purposes. Since the Stage 1 mixer has a double-balanced design, there is high rejection of local-oscillator and RF input signals at the mixer output. However, the filter needs to supply DC bias to the Stage 1 mixer output, and for this reason it is crucial to ensure that the IF filter Vcc is well decoupled over a wide frequency range. A decoupling inductor is used to achieve this (L3 = 680nH) in conjunction with wide-band decoupling capacitors (C6 = 10pF, C5 = 1nF, and C4 = 47nF).

The layout of the filter on a PCB is fairly critical, since any change in separation of the components can affect inter-component parasitics, and hence the response of the filter. It is worth ensuring that balanced signal tracks are kept close together and have the same length for each of the two signal lines. Allowance should be made to ensure there is good isolation between the filter and the RF input signal track.

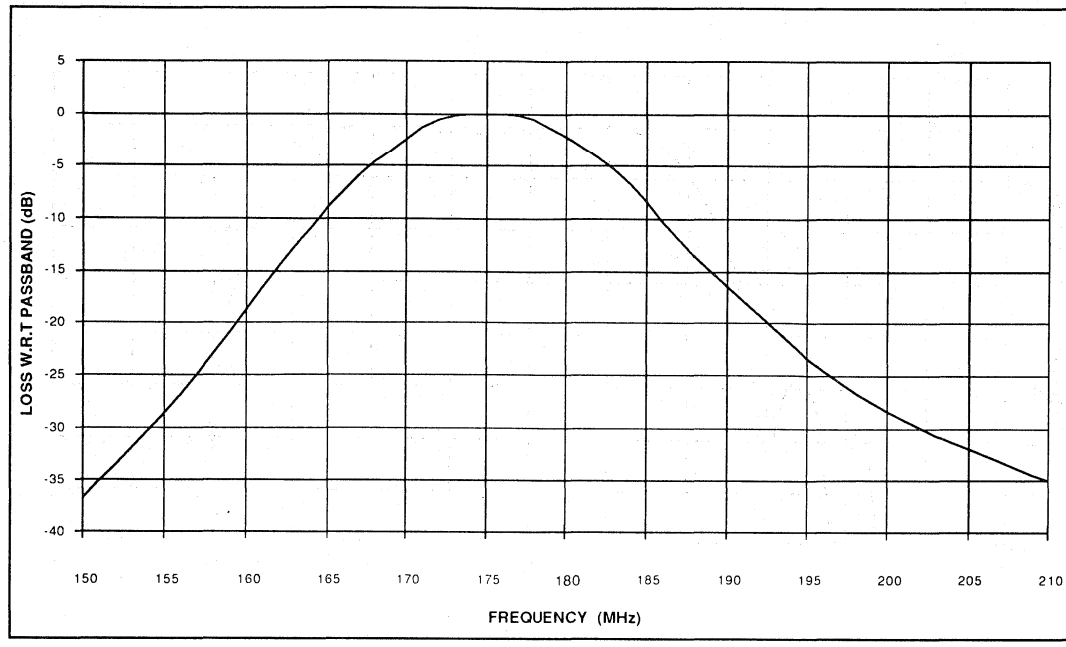


Fig.14 Typical frequency response of 1st IF filter

2nd IF filter

Centre Frequency	35.42MHz
Pass Band	±1.0MHz (within ±1.0dB)
Insertion loss	3 to 18dB
Stop Band	>10dB within ±2.0MHz
3rd IF Image frequency at 2nd IF	26.8MHz
Group-delay ripple	<300ns (34.62 to 36.22MHz)
Maximum group-delay	<1.7µs
Source Impedance	500Ω typical
Load Impedance	1000Ω typical

The second external IF filter is connected between the output of Stage 2 and input of Stage 3. It is required to define the bandwidth of the RF section of the GPS receiver. Hence it is critical to the receiver performance. The filter should be flat across the 2MHz bandwidth of the GPS Coarse Acquisition (C/A) code signal. It should also have high rejection (greater than 20dB) beyond this bandwidth, and so should have a brick-wall type response at these extremes. This can be realised with a specifically designed SAW filter, the DW9255, available from GEC Plessey Semiconductors, (refer to Data-Sheet number DS3861).This SAW filter provides a 1dB Bandwidth of typically 1.9MHz centred on 35.42MHz, with a typical pass band ripple of 0.8dB, when the SAW input and output capacitance is resonantly matched with inductors of optimum value. The out-of-band signal rejection is better than 21dB at ±2.0MHz, and better than 35dB at ±7.5MHz.

The frequency response of the DW9255 SAW filter with matching components is shown in Fig.15.

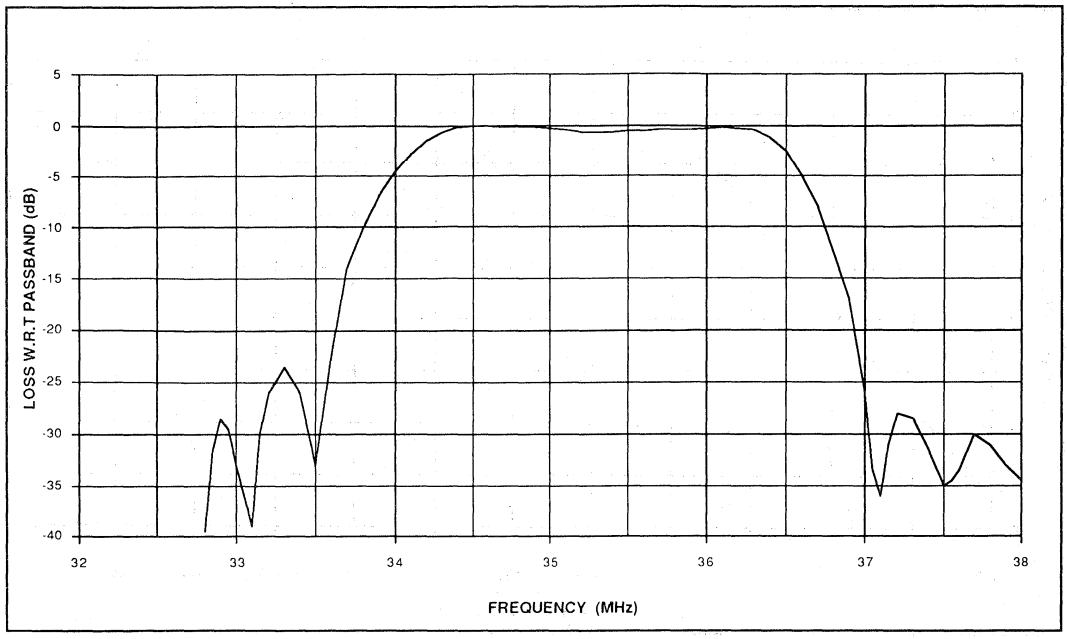


Fig.15 Typical frequency response of DW9255 SAW filter used as 2nd IF filter

3rd IF filter

Centre Frequency	4.3MHz
Pass Band	see GP2015 data sheet DS4374 - "Electrical characteristics"

The third IF filter is on-chip on the GP2015, and so cannot be user-defined. The performance of this filter is defined in the data-sheet. The overall RF bandwidth of the GPS receiver is defined by the 2nd IF filter, so the third IF filter is used to reject out-of-band noise and interference from entering the on-chip analog to digital converter. The response is essentially band pass, with a low pass operating above 10MHz, and a high-pass filter with a corner frequency of 2.0MHz which is used between the point which the IFOUT signal is connected, and the analog to digital converter. Hence, the IFOUT signal will NOT show the high-pass response.

The final IF can be monitored via the IFOUT test-point before the signal is digitised. This test-point is a high-impedance output, buffered by an on-chip 1kΩ resistor. To monitor this point, it is imperative that the signal is AC coupled, since there is a DC bias from the GP2015.

The frequency response of the third IF filter is shown in Fig.16, with 3 traces:-

IFOUT RESPONSE - spectrum observed at IFOUT pin,

ZERO RESPONSE - response calculated between IFOUT pin and analog to digital converter,

ADC I/P RESPONSE - IF spectrum of stage 3 calculated at analog to digital converter input.

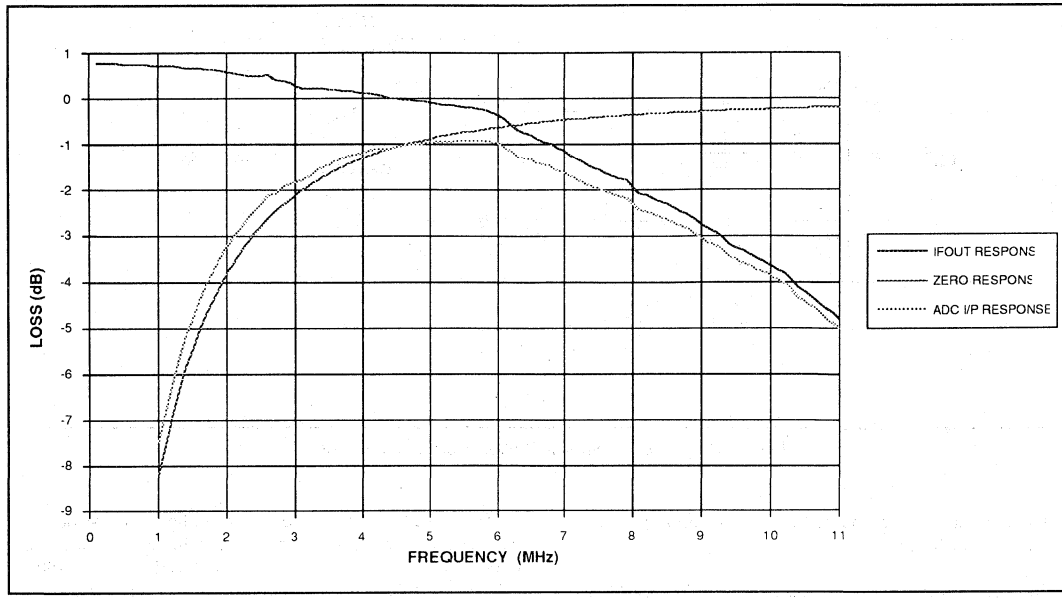


Fig.16 Typical frequency response of 3rd IF filter (on-chip)

AGC TIME CONSTANT AND MONITORING OF GAIN LEVEL

The third IF stage of the GP2015 has an Automatic Gain Control (AGC) to ensure that the level of the IF signal at the input to the Analog to Digital converter remains constant, giving a duty-cycle for the MAG data output of 30%.

In most applications, the time-constant (Δt) of the AGC can be fixed to approximately 2ms with the connection of a 100nF capacitor between pins AGC+ (pin 22) and AGC- (pin 21). However, there are now applications using "pseudolites" for aircraft landing systems where the AGC will need to have a much shorter time-constant, maybe in the order of 50µs, to cope with the huge difference in RF signal level from these and the satellites in the sky.

The time-constant of the AGC with a given capacitor ($Cagc$) connected between AGC+ and AGC- is dependent on the required gain change.

The ratio of gain adjustment ($\Delta Gain$) to the change of voltage across the AGC capacitor ($\Delta Vagc$) is approximately 400dB/V. (Although NOT linear over the whole gain adjustment range, 0.4dB/mV is a reasonable approximation).

For the case of a large interfering signal (in close proximity to a pseudolite, for example) driving the AGC to reduce gain, the recovery time after the interfering signal disappears depends upon the rate of change of $\Delta Vagc$. For large gain changes the AGC capacitor is charged/discharged by a 50µA current.

$$\frac{\Delta Vagc}{\Delta t} = \frac{50\mu A}{Cagc} \qquad \therefore \Delta t = \frac{Cagc \times \Delta Gain}{400 \times (50 \times 10^{-6})}$$

For example, a 40dB change in gain gives:-

$$\Delta Vagc = 100mV \text{ and } \Delta t = 2000 \times Cagc$$

The level of gain reduction by the AGC can be monitored by measuring the change in differential voltage across the AGC capacitor (Cagc). This voltage can also be used to drive a differential amplifier to give a voltage change with respect to 0V (Vee), see fig.17.

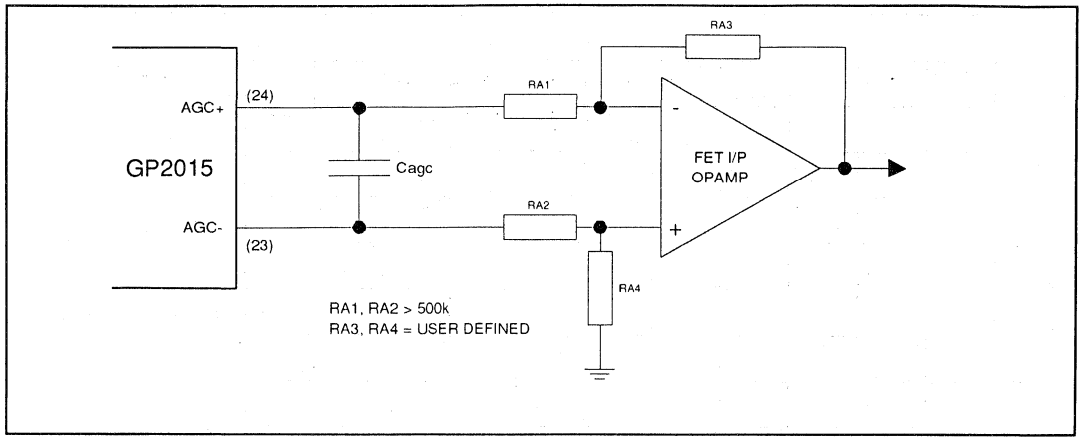


Fig.17 A differential amplifier buffer used to monitor AGC

The following points should be noted when applying this circuit to the GP2015:-

1) The output DC bias on AGC+ (pin 24) and AGC- (pin 23) can vary from Vcc to (Vcc-0.4V) maximum. The op amp should have the capability of measuring these DC voltages with a high common-mode-rejection-ratio (CMRR).

2) The load impedance of the differential amplifier must be *greater* than 1MΩ, to ensure the AGC performance is NOT affected.

3) An op amp with a very-low input offset current should be used (e.g FET input).

This circuit will *not* provide an indication of received GPS signal power, because this is buried in the background noise over a 2MHz bandwidth. A change in AGC differential voltage will provide an indication of jamming signals and whether the front-end LNA (connected between the antenna and GP2015) is operating. Fig.18 shows how the voltage on AGC+ (pin24) varies with respect to the voltage on AGC- (pin23), when a CW signal at 1575.42MHz is applied to the RF input of a GP2015.

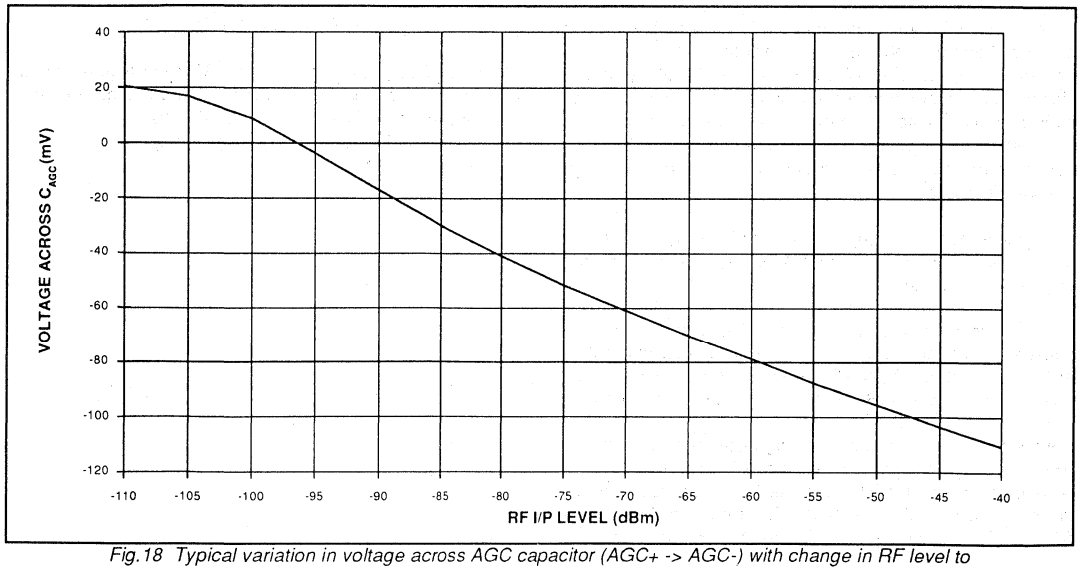


Fig.18 Typical variation in voltage across AGC capacitor (AGC+ -> AGC-) with change in RF level to GP2015 - typical at 25°C

GP2015 JAMMING SUSCEPTIBILITY

The GP2015 uses a triple-conversion frequency plan to provide a superior anti-jamming performance. The L band is increasingly being used for more RF applications besides GPS and so it will become more congested with GPS hostile signals.

The method used for showing the effects of a jamming signal applied to the RF Input of a GP2015 was to 'sweep' a jamming signal of a known power level across a pre-determined frequency spectrum combined with a GPS signal from a GPS active antenna. The GP2015 was configured as part of a complete receiver known as GPSBuilder-2.1, which operates with an IBM-compatible personal computer. In this configuration, the signal-to-noise ratio of a correlated GPS signal could be monitored whilst the jamming signal frequency was swept. The RF configuration used for this experiment is shown in fig.19.

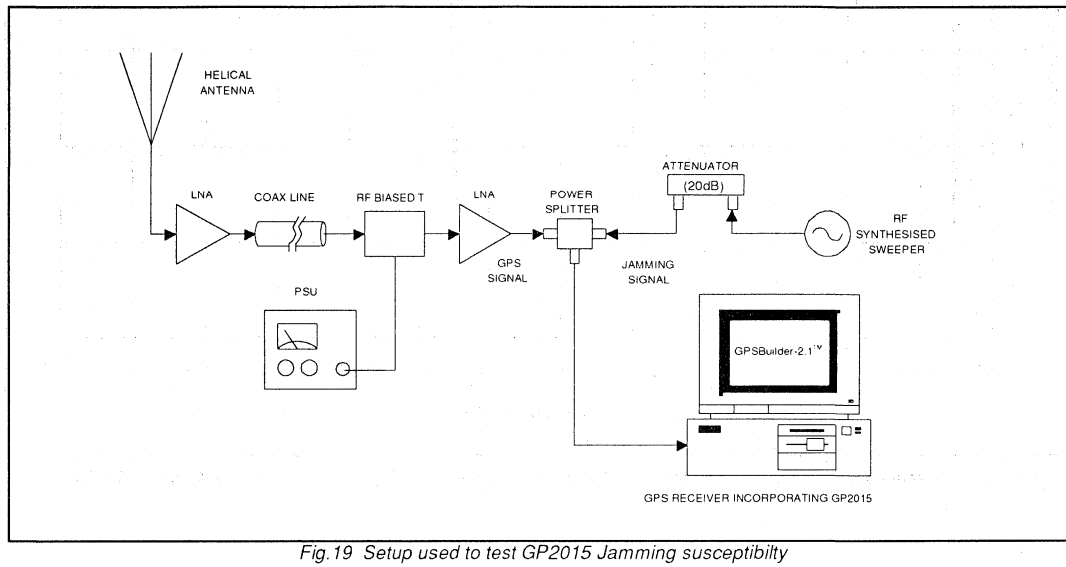


Fig.19 Setup used to test GP2015 Jamming susceptibilty

GPSBuilder-2.1 is available from GEC Plessey Semiconductors (refer to GPSBuilder-2.1 Product Brief No. DS4537).

A -40dBm signal (which simulates a very high level jamming signal) was swept from 1200MHz to 1850MHz to highlight any areas of susceptibility to jamming, with the effects being visible from the data logged Signal to Noise Ratio (SNR) from GPSBuilder-2.1. The plot in fig. 20 shows the SNR of the GPS data from a satellite known to be in a well elevated position in the sky, and the effect of the swept jamming signal across a 1200 to 1850MHz frequency range.

Note that the GPS data SNR is very poor when the jammer is at 1224.58MHz (the image frequency of 1575.42MHz). In fact the receiver loses the GPS data completely in this instance. This is due to the AGC in Stage 3 adjusting the gain for the jamming signal, and so the noise in which the GPS data is buried will see insufficient gain in the GP2015 to give a valid data output. Also, the Stage 2 mixer will go into gain compression. The same is also true when the jammer is at 1575.42MHz which is the L1 band signal frequency.

The plot in fig.20 should be used as a guide for when the GP2015 is likely to encounter interference signals (e.g. from mobile phones (PDC)). The jamming resistance is very good unless jamming signals appear at the following frequencies (within ±3MHz):-

1224.58MHZ
1295.42MHz
1435.42MHz
1504.58MHz
1575.42MHz

All these frequencies produce a component at the IFOUT (pin 1) at a frequency of 4.309MHz

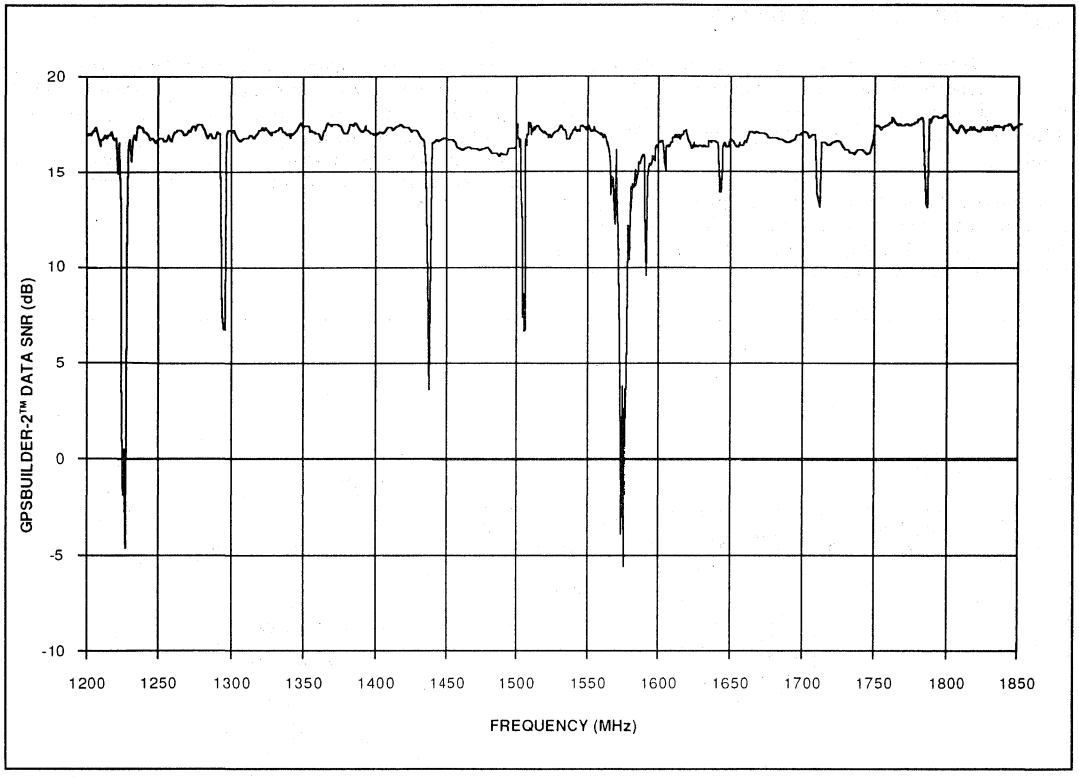


Fig.20 Correlated GPS data Signal to Noise with a swept -40dBm Jamming signal across 1200MHz to 1850MHz

An interference signal at 1224.58MHz is unlikely due to its closeness to the L2 band GPS signal frequency at 1227.6MHz.

There is a dip in the response at 1504.58MHz, because this frequency mixes down to 104.58MHz at the first IF, where it becomes the image of the second IF. 1295.42MHz similarly mixes down to 104.58MHz at the first IF. The effect of both frequencies can be reduced by increasing the rejection of the first IF filter at 104.58MHz.

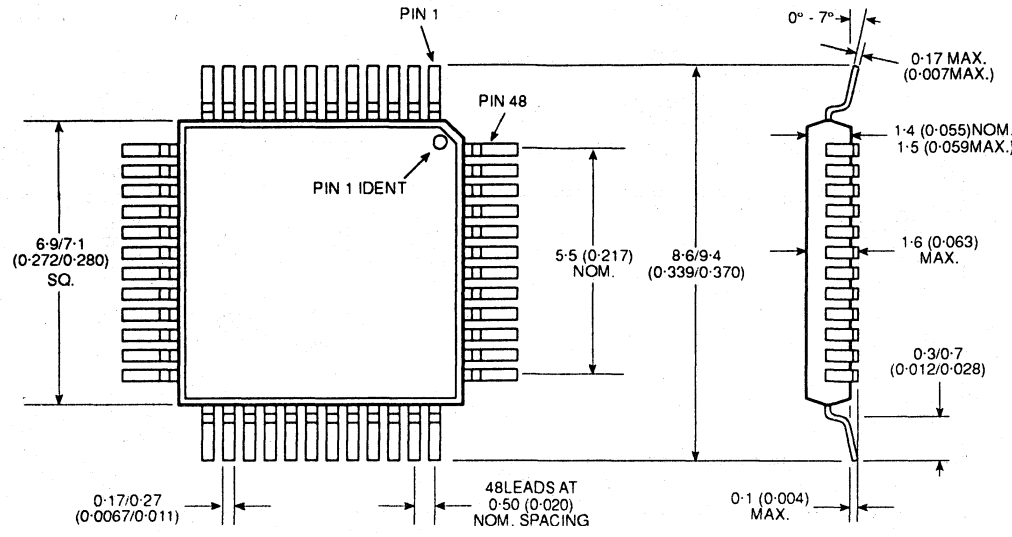
In any application where high-energy, out-of-band interference signals are expected at the RF i/p (pin 29) of the GP2015, it is best to try and filter out the signals before they enter the RF I/P. This can be achieved by cascading multi-pole ceramic filters in the RF signal line. It is vital that the amplitude of any RF interference signal is kept well below the minimum specification for Mixer 1 1dB Gain Compression (10dB below gives good margin) - refer to GP2015 datasheet - Electrical Characteristics. Otherwise, the GP2015 will gain -compress on the interference signal, and hence gain-compress the wanted GPS signal.

Section 6
Package Outlines

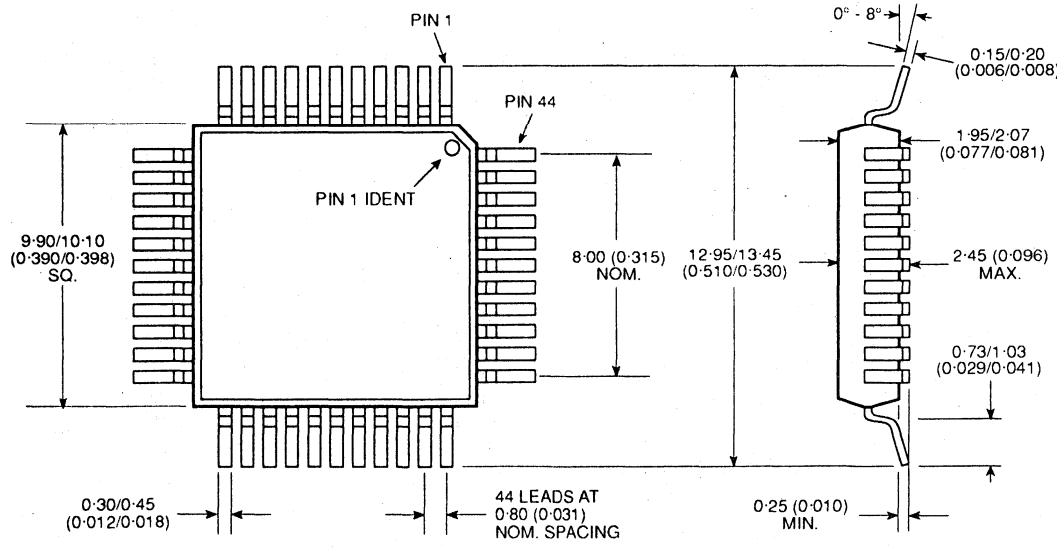
NOTES

1. Dimensions are shown thus: mm (in).
2. Unless otherwise indicated, controlling dimensions are in inches.
3. All package outline diagrams are for guidance only. Please contact you nearest GEC Plessey Semiconductors Customer Service Centre for further information.

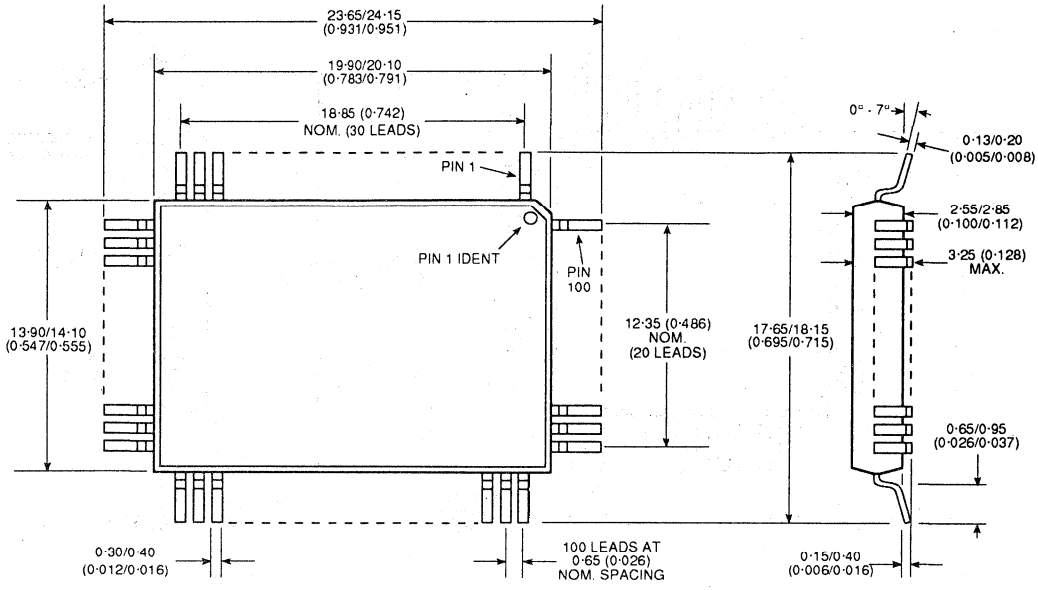
GEC PLESSEY
SEMICONDUCTORS



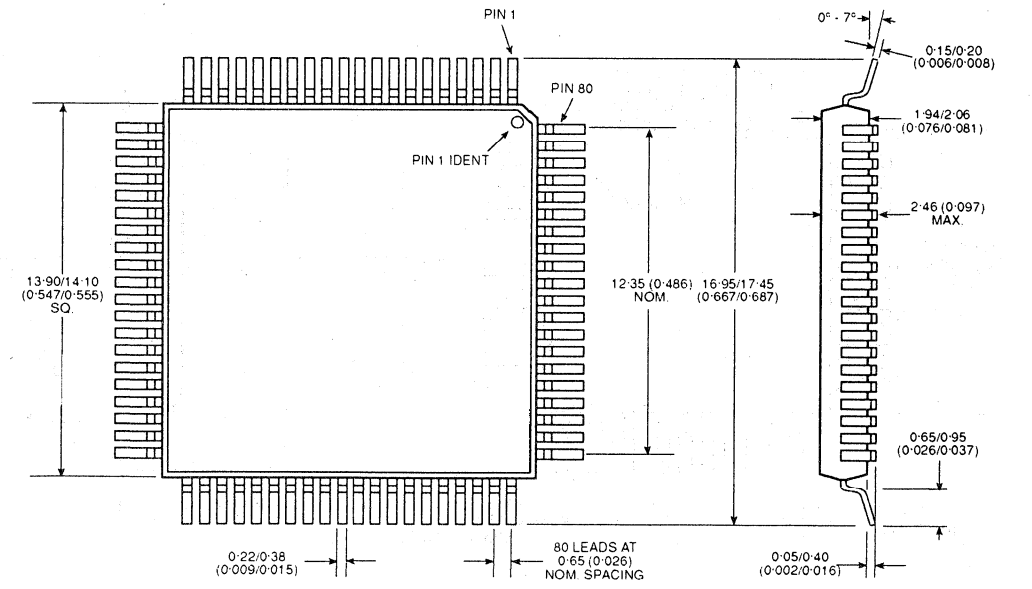
48-LEAD FINE PITCH PLASTIC QUAD FLATPACK - FP48



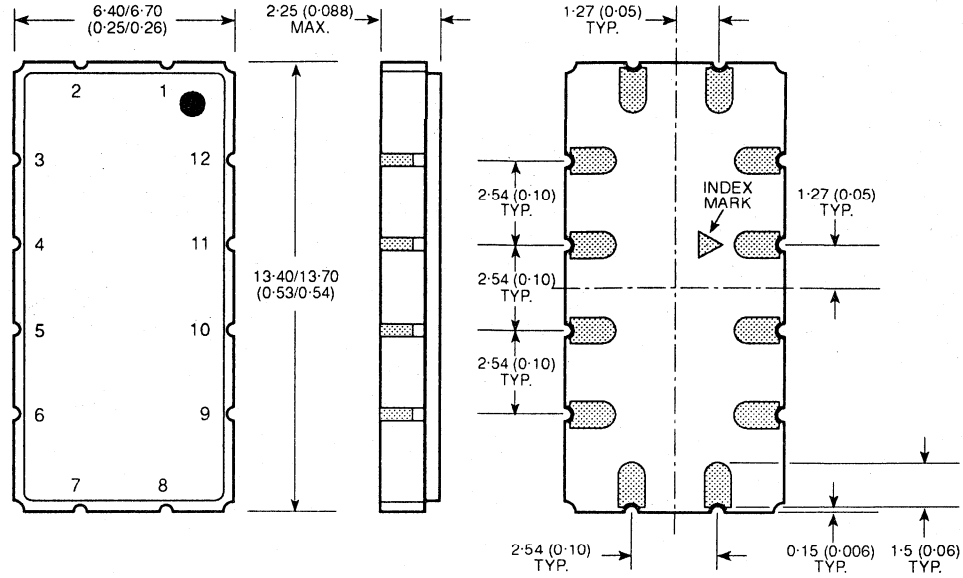
44-LEAD PLASTIC QUAD FLATPACK - GP44



100-LEAD PLASTIC QUAD FLATPACK (RECTANGULAR) - GP100/R



80-LEAD PLASTIC QUAD FLATPACK - GQ80



12-PAD LEADLESS CHIP CARRIER (SEAM SEAL) - LCS12/1

Section 7

GEC Plessey Semiconductors Locations

Key: CS = Customer Services, D = Distributor, PO = Power Products Only, R = Representative, SD = ASIC Design.

FRANCE & BENELUX

CS SD **GEC Plessey Semiconductors,** Z.A. Courtaboeuf, Miniparc 6, Avenue des Andes, Bât. 2-BP 142, 91944, Les Ulis Cedex A. **France.** Tel: (1) 69 18 90 00. Fax: (1) 64 46 06 07.

CS PO **GEC Plessey Semiconductors,** 2 rue Henri-Bergson, 92665 Asnieres Cedex, **France.** Tel: (1) 40 80 54 00. Fax: (1) 40 80 55 87 ■ Griensven 10, Den Dungen, (N. Br.), 5275KE, **Netherlands.** Tel: 73 594 1107. Fax: 73 594 1119.

D **Omnitech Sertronique, France:** C.A. de Monthéard, 11 rue Edgar Brandt, 72016 Le Mans CEDEX. Tel: 43 86 74 74. Fax: 43 86 74 86 ■ 165 boulevard de Valmy, Evolic Batiment 1, 92706 Colombes. Tel: 1 46 13 07 80. Fax: 1 46 13 07 90 ■ Z.I. Prairie de Mauves, 64, Rue de l'Etrier, BP7405, 44074 Nantes CEDEX 03. Tel: 40 49 90 90. Fax: 40 68 06 72 ■ 99 boulevard de l'Artillerie, 69007 Lyon. Tel: 72 73 11 87. Fax: 72 73 18 00 ■ 37 rue Saint-Eloi, 76000 Rouen. Tel: 35 88 00 38. Fax: 35 15 06 22 ■ 20 rue Cabanis, 59041 Lille. Tel: 20 43 96 44. Fax: 20 56 00 49 ■ Parc Cadera Sud, Batiment F, 33700 Bordeaux Merignac. Tel: 56 34 46 00. Fax: 56 34 47 13.

D **3D, France:** 6-8 rue Ambroise Croisat, Z.I. des Glaises, 91120 Palaiseau. Tel: 1 64 47 29 29 Fax: 1 64 47 00 84 ■ 3 rue Berthelot, 69627 Villeurbanne CEDEX. Tel: 72 35 22 00. Fax: 72 34 67 72 ■ Z.I. du terroir, rue de l'industrie, 31140 Saint Alban. Tel: 61 37 44 00. Fax: 61 37 44 29 ■ Parc Club du golf, Batiment 1, 13856 Aix-en-Provence CEDEX 3. Tel: 42 16 77 88. Fax: 42 39 4728 ■ 1 rue de la Faisandereie, Bat B1 P.C. de Tanneries, F-67883 Tanneries CEDEX. Tel: 88 77 26 46. Fax: 88 76 13 30 ■ 6 rue Abbe Henri Gregoire, F-35000 Rennes. Tel: 99 32 44 33. Fax: 99 51 33 93 ■ 22 rue de Seclin, F-59175 Vendeville. Tel: 20 62 07 67. Fax: 20 62 07 66.

D **Tekelec-Airtronic BV,** Postbus 63, Industrieweg 8A, 2700 AB Zoetermeer, **Netherlands.** Tel:0793 310100. Fax: 0793 417504

D **ACAL NV,** Lozenberg 4, B-1932 Zaventem, **Belgium.** Tel: (2) 7205983. Fax: (2) 7254815.

PO R **Manudax NV,** Avenue Du Laerbeeklaan 74, 1090 Bruxelles, **Belgium.** Tel: 02 477 9322. Fax: 02 477 9320.

GERMANY, AUSTRIA & SWITZERLAND

CS SD **GEC Plessey Semiconductors,** Ungererstraße 129, 80805 München, **Germany.** Tel: 089/36 0906-0. Fax: 089/36 0906-55

D **AS Electronic Vertriebs GmbH,** In den Gaerten 2, D-61352 Bad Homburg, **Germany.** Tel: 06172 458931. Fax: 06172 42000.

D **Farnell Electronic Services GmbH,** Bahnhofstrasse 44, D-71696 Moeglingen, **Germany.** Tel: 071 41 4870. Fax: 07141 487210.

D **Micronetics GmbH,** Dieselstrasse 12, D-71272 Renningen, **Germany.** Tel: 07159 925830. Fax: 07159 9258355.

D **Weisbauer Elektronik GmbH,** Heiliger Weg 1, D-44135 Dortmund, **Germany.** Tel: 0231 579547. Fax: 0231 577514.

D **Eurodis Electronics GmbH,** Lamezanstrasse 10, A-1232 Wien, **Austria.** Tel: 1 610620. Fax: 1 61062151.

PO R **Novatronic GmbH,** Goergengasse 27/5, A-1190 Wien, **Austria.** Tel: 1 325 548. Fax: 1 325 513.

D **Basix AG,** Hardturmstr 181, CH-8010 Zuerich, **Switzerland.** Tel: 1 2761111. Fax: 1 2761234.

PO R **Schlesser Electronic AG,** Industrievertretungen, Hardstrasse 41, CH-5430 Wettingen, **Switzerland.** Tel: 056 4271 127. Fax: 056 4272 525.

ITALY

CS **GEC Plessey Semiconductors,** Via Fosse Ardeatine, N4, 20092 Cinisello Balsamo (MI). Tel: (02) 6607151. Fax: (02) 66040993.

D **Avnet EMG. S.r.l., Divisione Adelsy,** Via Novara 570, 20153 Milano. Tel: 02 381901. Fax: 02 38002988.

D **Eurelettronica SpA,** Via E. Fermi 8, 20090 Assago (MI). Tel: 02 457841. Fax: 02 4880275.

D **Eurodis Fanton Srl,** Via Melegnano, 22, 20019 Settimo Milanese (MI). Tel: 02 48912963. Fax: 02 4597913.

PO R **Sisram SpA,** Casella Postale 1168, 10100 Torino. Tel: 011 4331782/3/4. Fax: 011 4336521.

JAPAN

CS SD **GEC Plessey Semiconductors,** CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.

D **Cornes & Company Ltd:** Ryukakusan Building, 2-5-12, Higashi Kanda, Chiyoda-ku,Tokyo 101. Tel: 3-5821-1628. Fax: 3-5821-1632 ■ 1-13-40 Nishi-hommachi, Nishi-ku, Osaka 550. Tel: 6 532 1012. Fax: 6 532-7749.

KOREA

CS **GEC Plessey Semiconductors,** 4th Floor, Cheonwoo Building, 736 Yogsam-Dong, Kangnam-Ku, Seoul 135-080. Tel: (2) 5668141. Fax: (2) 5697933

D **KML Corporation,** 6th Floor, Dukmyung Building, (A-Dong) 113-3, Banpo-Dong, Shucho-Gu, CPO Box 7981, Seoul. Tel: (02) 595 9101-6. Fax: (02) 595 9107.

PO R **Bochang Trading Corporation,** Room 1616, Samkoo Building, 16-49, Hangangro 3 Ka, Yongsan-Ku, Seoul. Tel: (02) 705 0890. Fax: (02) 705 1891.

		GEC Plessey Semiconductors, P O Box 660017, 1500 Green Hills Road, Scotts Valley, CA 95067-0017, **USA.** Tel: (408) 438 2900. Fax: (408) 438 7023/5576
CS		**GEC Plessey Semiconductors,** 3608 Boul. St. Charles, Suite 9, Kirkland, Quebec, H9H 3C3, **Canada.** Tel: (514) 697-0095. Fax: (514) 694-7006 ■ 4635 South Lakeshore Drive, Tempe, AZ 85282, **USA.** Tel: (602) 491-0910. Fax: (602) 491-1219 ■ 7935 Datura Circle West, Littleton, CO 80120, **USA.** Tel: (303) 798-0250. Fax: (303) 730-2460 ■ 9540 Behner Lane, Indianapolis, IN 46250, **USA.** Tel: (317) 845-7332. Fax: (317) 577-9344. ■ 13 Tamwood Lane, Sewell, NJ 08080, **USA.** Tel: (609) 582-2280. Fax: (609) 582-6397. ■ 9330 LBJ Freeway, Ste. 665, Dallas, TX 75243, **USA.** Tel: (214) 690-4930. Fax: (214) 680-9753.
CS SD		**GEC Plessey Semiconductors,** 2600 Michelson Drive, Suite 830, Irvine, CA 92715, **USA.** Tel: (714) 852-3900. Fax: (714) 852-3910 ■ 1735 Technology Drive, Suite 240, San Jose, CA 95110, **USA.** Tel: (408) 451-4700. Fax: (408) 451-4710 (CS)/(408) 451-4715 (SD) ■ 3 Allied Drive, Suite 125, Dedham, MA 02026, **USA.** Tel: (617) 251-0100. Fax: (617) 251-0104.
CS PO		**GEC Plessey Semiconductors,** 50 Lambie Circle, Portsmouth, RI 02871, **USA** Tel: (401) 683-4038. Fax: (401) 683-4218 ■ 3365 Hollywood Lane, Brookfield, WI 53045, **USA.** Tel: (414) 781-3922. Fax: (414) 781-9722.
Canada	R	**GM Assoc. Inc.,** Calgary, Alberta, Tel: (403) 275-7178. Fax: (403) 274-6355 ■ Vancouver, BC, Tel: (604) 439-3383. Fax: (604) 439-8479 ■ St. Laurent, Quebec, Tel: (514) 335-9572. Fax: (514) 335-9573 ■ Mississauga, Ontario, Tel: (905) 671-8111. Fax: (905) 671-2422 ■ Nepean, Ottawa, Tel: (613) 820-3822. Fax: (613) 820-7633.
	PO R	**Leister Blake Enterprises Ltd,** West Vancouver, BC, Tel: (604) 926-6127. Fax: (604) 926-0372. ■ **Power-Teck,** Mississauga, Ontario, Tel: (905) 858-0340. Fax: (905) 858-0214.
	D	**Insight Electronics,** Richmond, BC, Tel: (604) 270-3232. Fax: (604) 270-3356 ■ Etobicoke, Ontario, Tel: (416) 622-7006. Fax: (416) 622-5115 ■ Ottawa, Ontario, Tel: (613) 233-1799. Fax: (613) 233-2843 ■ Dorval, Quebec, Tel: (514) 421-7373. Fax: (514) 421-0024 ■ **Pioneer Standard,** Calgary, Alberta, Tel: (403) 291-1988. Fax: (403) 291-0740 ■ Richmond, BC, Tel: (604) 273-5575. Fax: (604) 273-2413 ■ Ste-Foy, Quebec, Tel: (418) 654-1077. Fax: (418) 654-2958 ■ Ville St. Laurent, Tel: (514) 737-9700. Fax: (514) 737-5212 ■ Nepean, Ontario, Tel: (613) 226-8840. Fax: (613) 226-6352 ■ Mississauga, Tel: (905) 405-8300. Fax: (905) 405-6423.
USA, AL	R	**Electramark,** Huntsville, Tel: (205) 533-5445. Fax: (205) 533-5455
	D	**Insight Electronics,** Huntsville, Tel: (205) 830-1222. Fax: (205) 830-1225 ■ **Pioneer Standard,** Huntsville, Tel: (205) 837-9300. Fax: (205) 837-9358
USA, AZ	R	**Fred Board Associates,** Scottsdale, Tel: (602) 994-9388. Fax: (602) 994-9477 ■ Tucson, Tel: (520) 797-7746. Fax: (520) 797-1552.
	D	**Alliance,** Scottsdale, Tel: (602) 483-9400. Fax: (602) 443-3898. ■ **Insight Electronics,** Tempe, Tel: (602) 829-1800. Fax: (602) 967-2658 ■ **Pioneer Standard,** Tempe, Tel: (602) 350-9335. Fax: (602) 350-9376
USA, CA	R	**Gary Chilcote & Associates,** Fallbrook, Tel: (619) 728 7678. Fax: (619) 728 3738. ■ **Jones & McGeoy,** Newport Beach, Tel: (714) 724 8080. Fax: (714) 724 8090.
	PO R	**Maxim Electronic Sales,** Milpitas, Tel: (409) 946-6001. Fax: (409) 946-6007 ■ **Van Gott & Associates,** Arcadia, Tel: (818) 445-9728. Fax: (818) 445-5019 ■ San Diego, Tel: (619) 489-1893. Fax: (619) 489-8167.
	D	**Insight Electronics,** Irvine, Tel: (714) 727-3291. Fax: (714) 727-1804 ■ San Diego, Tel: (619) 677-3100. Fax: (619) 677-3131 ■ Sunnyvale, Tel: (408) 720-9222. Fax: (408) 720-8390 ■ Westlake Village, Tel: (818) 707-2101. Fax: (818) 707-0321 ■ **Pioneer Standard,** Agoura Hills, Tel: (818) 865-5800. Fax: (818) 865-5814 ■ Irvine, Tel: (714) 753-5090. Fax: (714) 753-5074 ■ San Diego, Tel: (619) 514-7700. Fax: (619) 514-7799 ■ San Jose, Tel: (408) 954-9100. Fax: (408) 954-9113
USA, CO	D	**Insight Electronics,** Engelwood, Tel: (303) 649-1800. Fax: (303) 649-1818
USA, CT	R	**Stone Components,** Chester, Tel: (508) 383-0119. Fax: (203) 526-2231
	PO R	**MPS Electronics,** Meriden, Tel: (203) 235-1414
	D	**Pioneer Standard,** Shelton, Tel: (203) 929-5600. Fax: (203) 929-9791
USA, FL	R	**American Micro Sales,** Casselberry, Tel: (407) 831 2505. Fax: (407) 831 1842 ■ Clearwater, Tel: (813) 724-1980. Fax: (813) 724-3984 ■ Deerfield Beach, Tel: (305) 421-9077. Fax: (305) 421-8387
	D	**Insight Electronics,** Altamonte Springs, Tel: (407) 834-6310. Fax: (407) 834-6461 ■ Boca Raton, Tel: (407) 997-2540. Fax: (410) 997-2542 ■ Clearwater, Tel: (813) 524-8850. Fax: (813) 532-4252 ■ **Pioneer Standard,** Altamonte Springs, Tel: (407) 834-9090. Fax: (407) 834-0865 ■ Deer Field Beach, Tel: (305) 428-8877. Fax: (305) 481-2950
USA, GA	R	**Electramark,** Norcross, Tel: (770) 446-7915. Fax: (770) 263-6389.
	PO R	**Benchmark Technical Sales Inc.,** Atlanta, Tel: (404) 446-1711. Fax: (404) 446-2854
	D	**Insight Electronics,** Duluth, Tel: (404) 717-8566. Fax: (404) 717-8588 ■ **Pioneer Standard,** Duluth, Tel: (404) 623-1003. Fax: (404) 623-0665
USA, IA	R	**Lorenz Sales, Inc.,** Cedar Rapids, Tel: (319) 294-1000. Fax: (319) 294-1111
USA, IL	R	**Micro Sales, Inc.,** Itasca, Tel: (708) 285-1000. Fax: (708) 285-1008
	PO R	**DAB Electronics,** Wood Dale, Tel: (708) 595-9210. Fax: (708) 595-9212
	D	**Insight Electronics,** Schaumburg, Tel: (708) 885-9700. Fax: (708) 885-9701 ■ **Pioneer Standard,** Addison, Tel: (708) 495-9680. Fax: (708) 495-9831
USA, IN	R	**Leslie M. DeVoe,** Indianapolis, Tel: (317) 842-3245. Fax: (317) 845-8440.
	D	**Pioneer Standard,** Indianapolis, Tel: (317) 573-0880. Fax: (317) 573-0979
USA, KS	R	**Lorenz Sales, Inc.,** Overland Park, Tel: (913) 469-1312. Fax: (913) 469-1238 ■ Wichita, Tel: (316) 721-0500. Fax: (316) 721-0566
	D	**Insight Electronics,** Lenexa, Tel: (913) 492-0408. Fax: (913) 492-0708
USA, MA	R	**Stone Components,** Framingham, Tel: (508) 875-3266. Fax: (508) 875-0537 ■ Newburyport, Tel: (508) 462-1079. Fax: (508) 462-8948. Voicemail: (508) 383-0113.
	PO R	**MPS Electronics,** Norwood, Tel: (617) 769-8700. Fax: (617) 769-7703.
	D	**Insight Electronics,** Burlington, Tel: (617) 270-9400. Fax: (617) 270-3279 ■ **Pioneer Standard,** Lexington, Tel: (617) 861-9200. Fax: (617) 863-1547
USA, MD	R	**Walker Associates,** Mitchellville, Tel: (301) 249-7145. Fax: (301) 390-1833 ■ Westminster, Tel: (410) 876-9399. Fax: (410) 876-9285.
	PO R	**Callas Electronics,** Ellicott City, Tel: (410) 465-0044. Fax: (410) 465-0045.

	D	**Insight Electronics,** Columbia, Tel: (410) 381-3130. Fax: (410) 381-3141 ■ **Pioneer Standard,** Gaithersburg, Tel: (301) 921-0660. Fax: (301) 921-4255
USA, MI	R	**Greiner Associates Inc.,** Grosse Point Park, Tel: (313) 499-0188. Fax: (313) 499-0665.
	D	**Insight Electronics,** Brighton, Tel: (810) 229-7710. Fax: (810) 229-6435 ■ **Pioneer Standard,** Plymouth, Tel: (313) 416-2157. Fax: (313) 427-2415
USA, MN	R	**High Technology Sales,** Bloomington, Tel: (612) 844-9933. Fax: (612) 844-9930.
	D	**Insight Electronics,** St. Louis Park, Tel: (612) 525-9999. Fax: (612) 525-9998 ■ **Pioneer Standard,** Eden Prairie, Tel: (612) 944-3355. Fax: (612) 944-3794
USA, MO	R	**Lorenz Sales, Inc.,** St. Louis, Tel: (314) 997-4558. Fax: (314) 997-5829
	PO R	**C. Logsdon & Associates,** St. Louis, Tel/Fax: (314) 843-6514.
	D	**Pioneer Standard,** St. Louis, Tel: (314) 542-3077. Fax: (314) 542-3078
USA, NC	PO R	**Benchmark Technical Sales Inc.,** Garner, Tel: (919) 773-0090. Fax: (919) 773-0780.
	D	**Pioneer Standard,** Morrisville, Tel: (919) 460-1530. Fax: (919) 460-1540.
USA, NE	R	**Lorenz Sales, Inc.,** Lincoln, Tel: (402) 475-4660. Fax: (402) 474-7094.
USA, NJ	R	**HLM Assoc.,** Parsippany, Tel: (201) 263-1535. Fax: (201) 263-0914
	PO R	**Compar,** Elerbon, Tel: (908) 229-3666. Fax: (908) 229-3687
	D	**Insight Electronics,** Marlton, Tel: (609) 985-5556. Fax: (609) 985-5895 ■ **Pioneer Standard,** Fairfield, Tel: (201) 575-3510. Fax: (201) 575-3454
USA, NY	R	**HLM Assoc.,** Northport, Tel: (516) 757-1606. Fax: (516) 757-1636. ■ **Omega Electronics, Inc.,** Webster, Tel: (716) 671 7822. Fax: (716) 671 7822. E-Mail: omegaks@aol.com/omegabb@aol.com
	PO R	**Compar,** Bellmore, Tel: (516) 221-7300. Fax: (516) 221-7600.
	D	**Mast,** Ronkonkoma, Tel: (516) 471-4422. Fax: (516) 471-2040. ■ **Pioneer Standard,** Binghamton, Tel: (607) 722-9300. Fax: (607) 722-9562 ■ Fairport, Tel: (716) 381-7070. Fax: (716) 381-5955 ■ Woodbury, Tel: (516) 921-8700. Fax: (516) 921-2143
USA, OH	R	**K.W. Electronic Sales, Inc.,** Dayton, Tel: (513) 890-2150. Fax: (513) 890-5408 ■ Shaker Heights, Tel: (216) 491-9177. Fax: (216) 491-9102
	PO R	**J. N. Bailey & Associates Inc.,** New Lebanon, Tel: (513) 687-1325. Fax: (513) 687-2930. ■ **Electronic Salesmasters Inc.,** Beachwood, Tel: (800) 544-4383/(216) 831-9555. Fax: (216) 831-8647.
	D	**Insight Electronics,** Gahanna, Tel: (614) 471-3801. Fax: (404) 471-3804 ■ Valley View, Tel: (216) 520-4333. Fax: (216) 520-4322 ■ **Pioneer Standard,** Cleveland, Tel: (216) 498-6503. Fax: (216) 587-3906 ■ Dayton, Tel: (513) 236-9900. Fax: (513) 236-8133
	PO D	**Darrah Electric,** Cleveland, Tel: (216) 631-0912. Fax: (216) 631-0440.
USA, OK	D	**Pioneer Standard,** Tulsa, Tel: (918) 665-7840. Fax: (918) 655-1891
USA, OR	R	**Venture Electronics,** Portland, Tel: (503) 624-0617. Fax: (503) 620-4682
	D	**Insight Electronics,** Beaverton, Tel: (503) 626-3103. Fax: (503) 641-4530
USA, PA	R	**K.W. Electronic Sales, Inc.,** Allison Park, Tel: (412) 492-0777. Fax: (412) 492-0780 ■ **Metz-Jade Associates, Inc.,** Wynnewood, Tel: (610) 896-7300. Fax: (610) 642-6293.
	D	**Pioneer Standard,** Pittsburgh, Tel: (412) 782-2300. Fax: (412) 963-8255 ■ Horsham, Tel: (215) 674-4000. Fax: (215) 674-3107
USA, PR	R	**American Micro Sales,** Rio Piedreas, Tel: (809) 274-1661. Fax: (809) 756-6152.
USA, TX	R	**O. & M. Sales,** Austin, Tel: (512) 453-0275. Fax: (512) 453-0088 ■ Dallas, Tel: (214) 361-8876. Fax: (214) 692-0235 ■ The Woodlands, Tel: (713) 894-5021. Fax: (713) 894-5022.
	D	**Insight Electronics,** Austin, Tel: (512) 719-3090. Fax: (512) 719-3091 ■ Houston, Tel: (713) 260-9614. Fax: (713) 260-9602 ■ Richardson, Tel: (214) 783-0800. Fax: (214) 680-2402 ■ **Pioneer Standard,** Austin, Tel: (512) 835-4000. Fax: (512) 835-9829 ■ Dallas, Tel: (214) 386-7300. Fax: (214) 490-6419 ■ Houston, Tel: (713) 495-4700. Fax: (713) 495-5642 ■ San Antonio, Tel: (210) 377-3440. Fax: (210) 378-3626
USA, UT	D	**Insight Electronics,** Salt Lake City, Tel: (801) 288-9001. Fax: (801) 288-9195
USA, WA	R	**Venture Electronics,** Bellevue, Tel: (206) 454-4594. Fax: (206) 454-9003.
	D	**Insight Electronics,** Kirkland, Tel: (206) 820-8100. Fax: (206) 821-2976
USA, WI	R	**Micro Sales, Inc.,** Brookfield, Tel: (414) 786-1403. Fax: (414) 786-1813.
	PO R	**DAB Electronics,** Brookfield, Tel: (414) 792-9870. Fax: (414) 792-9871.
	D	**Insight Electronics,** Wauwatosa, Tel: (414) 258-5338. Fax: (414) 258-5360. ■ **Pioneer Standard,** Brookfield, Tel: (414) 784-3480. Fax: (414) 784-3613.
USA, WV	PO R	**Burl Burgess,** Oak Hill, Tel: (304) 465-0742. Fax: (304) 465-8655.

SOUTH EAST ASIA & AUSTRALASIA

CS	**GEC Plessey Semiconductors,** No. 3 Tai Seng Drive, GEC Building, **Singapore** 1953. Tel: 3827708. Fax: 3828872
D	**GEC Electronics Division,** Unit 1, 38 South Street, Rydalmere, NSW 2116, **Australia.** Tel: 612 638 1888. Fax: 612 638 1798.
D	**Gain Tune Ltd,** Room 709, Oriental Building, 39 Jianshe Road, Shenzen, **China.** Tel: 755-2284970. Fax: 755-2284971. ■ Room 809, 8th Floor, Hunghom Commercial Centre, Tower B, 37-39 Ma Tau Wai Road, Hunghom, Kowloon, **Hong Kong.** Tel: 3654860. Fax: 7641129.
D	**World Peace Industrial Co Ltd,** Room 709, Oriental Building, 39 Jianshe Road, Shenzen, **China.** Tel: 755-2284970. Fax: 755-2284972.
D	**Mekaster Telecom PVT Ltd.,** 908 Ansal Bhawan, 16 Katuba Ghandi Marg, New Delhi, 100 001 **India** Tel: 11 3312110 Fax: 11 3712155.
PO R	**Usha (India) Ltd,** 12/1 Delhi-Mathura Road, Faridabad, 12003 (Haryana), **India.** Tel: 129 277641. Fax: 129 277679.
D	**Adequip Enterprise Sdn Bhd,** #6-01 6th Floor, Wisjma Stephens, 88 Jalan Raya Chulan, 50200 Kualar Lumpur, **Malaysia.** Tel: 2423522. Fax: 2423264.
PO R	**Choakchai Electronic Supplies Ltd,** Part. 128/22 Thanon, Corp. Atsadang, Bangkok 10200, **Thailand.** Tel: 2 223921. Fax: 2 2247639.
D	**Westech Electronics Co. Ltd,** 77/113 Moo Ban Kitikorn, Ladprao Soi 3, Ladprao Road, Ladyao, Jatujak, Bangkok 10900. **Thailand.** Tel: 2 5125531. Fax: 2 2365949.

SWEDEN

CS **GEC Plessey Semiconductors,** Katarina Bangata 79, 116 42 Stockholm. Tel: (08) 7029770. Fax: (08) 6404736.
PO R **Transemic International AB,** Box 2107, Egnahemswagen 21, 141 02 Huddinge. Tel: (08) 711 3404. Fax: (08) 746 7720.

TAIWAN, ROC

CS **GEC Plessey Semiconductors,** Room 503, 5F, 131 Min-Sheng E Road, Sec 3, Taipei. Tel: (02) 5461260. Fax: (02) 719 0260
D **Alltek Technology Corp.,** 3F, No. 108 Nan-King E Rd., Sec. 4, Taipei. Tel: 886-2-5790939. Fax: 886-2-5790936.
D **Serial Semiconductor Co., Ltd.,** 8F, No. 11, Lane 3, Tsao Ti Wei, Shen Keng Hsiang, Taipei Hsien. Tel: 886-2-6620088. Fax: 886-2-6629700.
PO R **Taiwan Thyristor Industries Co. Ltd,** 10F-5, No. 12, Lane 609, Chung-Hsin Road, Sec 5, San-Chung, Taipei. Tel: (02) 999 2101. Fax: (02) 999 2169.

UK

CS **GEC Plessey Semiconductors,** Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts, SN2 5AF. Tel: (01793) 726666. Fax: (01793) 518582.
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Publication No. HB4305 - 1.0 August 1996

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